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Very Large Scale Integration Algorithms And Architectures International Workshop Proceedings

Venkatesh Mahadevan, Jianhong Zhou



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Computer And Network Technology - Proceedings Of The International Conference On Iccnt 2009 Venkatesh

Mahadevan, Jianhong Zhou, 2009-07-16 ICCNT is the main annual computer and network research conference in Chennai that presents cutting edge research work. It will act as a platform for scientists, scholars, engineers, and students from universities all around the world to present ongoing research and hence foster better research relations between universities and the computer and networking industry.

Algorithms and Architectures for Cryptography and Source Coding in Non-Volatile Flash Memories Malek Safieh, 2021-08-09 In this work, algorithms and architectures for cryptography and source coding are developed which are suitable for many resource constrained embedded systems such as non-volatile flash memories. A new concept for elliptic curve cryptography is presented which uses an arithmetic over Gaussian integers. Gaussian integers are a subset of the complex numbers with integers as real and imaginary parts. Ordinary modular arithmetic over Gaussian integers is computationally expensive. To reduce the complexity, a new arithmetic based on the Montgomery reduction is presented. For the elliptic curve point multiplication, this arithmetic over Gaussian integers improves the computational efficiency, the resistance against side channel attacks, and reduces the memory requirements. Furthermore, an efficient variant of the Lempel Ziv Welch (LZW) algorithm for universal lossless data compression is investigated. Instead of one LZW dictionary, this algorithm applies several dictionaries to speed up the encoding process. Two dictionary partitioning techniques are introduced that improve the compression rate and reduce the memory size of this parallel dictionary LZW algorithm.

Microfluidic Very Large Scale Integration (VLSI) Paul Pop, Wajid Hassan Minhass, Jan Madsen, 2016-02-08 This book presents the state of the art techniques for the modeling, simulation, testing, compilation, and physical synthesis of mVLSI biochips. The authors describe a top-down modeling and synthesis methodology for the mVLSI biochips inspired by microelectronics VLSI methodologies. They introduce a modeling framework for the components and the biochip architecture and a high-level microfluidic protocol language. Coverage includes a topology graph-based model for the biochip architecture and a sequencing graph to model for biochemical application, showing how the application model can be obtained from the protocol language. The techniques described facilitate programmability and automation, enabling developers in the emerging large biochip market.

VLSI 2010 Annual Symposium Nikolaos Voros, Amar Mukherjee, Nicolas Sklavos, Konstantinos Masselos, Michael Huebner, 2011-09-08 VLSI 2010 Annual Symposium will present extended versions of the best papers presented in ISVLSI 2010 conference. The areas covered by the papers will include, among others: Emerging Trends in VLSI, Nanoelectronics, Molecular Biological and Quantum Computing, MEMS, VLSI Circuits and Systems, Field-programmable and Reconfigurable Systems, System Level Design, System on a Chip Design, Application Specific Low Power VLSI System Design, System Issues in Complexity, Low Power, Heat Dissipation, Power Awareness in VLSI Design, Test and Verification, Mixed Signal Design and Analysis, Electrical Packaging, Co-Design, Physical Design, Intellectual property creating and sharing.

Network-on-Chip Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

High Performance Computing for Big Data Chao Wang, 2017-10-16 High Performance Computing for Big Data Methodologies and Applications explores emerging high performance architectures for data intensive applications novel efficient analytical strategies to boost data processing and cutting edge applications in diverse fields such as machine learning life science neural networks and neuromorphic engineering The book is organized into two main sections The first section covers Big Data architectures including cloud computing systems and heterogeneous accelerators It also covers emerging 3D IC design principles for memory architectures and devices The second section of the book illustrates emerging and practical applications of Big Data across several domains including bioinformatics deep learning and neuromorphic engineering Features Covers a wide range of Big Data architectures including distributed systems like Hadoop Spark Includes accelerator based approaches for big data applications such as GPU based acceleration techniques and hardware

acceleration such as FPGA CGRA ASICs Presents emerging memory architectures and devices such as NVM STT RAM 3D IC design principles Describes advanced algorithms for different big data application domains Illustrates novel analytics techniques for Big Data applications scheduling mapping and partitioning methodologies Featuring contributions from leading experts this book presents state of the art research on the methodologies and applications of high performance computing for big data applications About the Editor Dr Chao Wang is an Associate Professor in the School of Computer Science at the University of Science and Technology of China He is the Associate Editor of ACM Transactions on Design Automations for Electronics Systems TODAES Applied Soft Computing Microprocessors and Microsystems IET Computers Digital Techniques and International Journal of Electronics Dr Chao Wang was the recipient of Youth Innovation Promotion Association CAS ACM China Rising Star Honorable Mention 2016 and best IP nomination of DATE 2015 He is now on the CCF Technical Committee on Computer Architecture CCF Task Force on Formal Methods He is a Senior Member of IEEE Senior Member of CCF and a Senior Member of ACM

Autonomic Networking-on-Chip Phan Cong-Vinh, 2018-09-03 Despite the growing mainstream importance and unique advantages of autonomic networking on chip ANoC technology Autonomic Networking On Chip Bio Inspired Specification Development and Verification is among the first books to evaluate research results on formalizing this emerging NoC paradigm which was inspired by the human nervous system The FIRST Book to Assess Research Results Opportunities Trends in BioChipNets The third book in the Embedded Multi Core Systems series from CRC Press this is an advanced technical guide and reference composed of contributions from prominent researchers in industry and academia around the world A response to the critical need for a global information exchange and dialogue it is written for engineers scientists practitioners and other researchers who have a basic understanding of NoC and are now ready to learn how to specify develop and verify ANoC using rigorous approaches Offers Expert Insights Into Technical Topics Including Bio inspired NoC How to map applications onto ANoC ANoC for FPGAs and structured ASICs Methods to apply formal methods in ANoC development Ways to formalize languages that enable ANoC Methods to validate and verify techniques for ANoC Use of self processes in ANoC self organization configuration healing optimization protection etc Use of calculi for reasoning about context awareness and programming models in ANoC With illustrative figures to simplify contents and enhance understanding this resource contains original peer reviewed chapters reporting on new developments and opportunities emerging trends and open research problems of interest to both the autonomic computing and network on chip communities Coverage includes state of the art ANoC architectures protocols technologies and applications This volume thoroughly explores the theory behind ANoC to illustrate strategies that enable readers to use formal ANoC methods yet still make sound judgments and allow for reasonable justifications in practice

Wireless Security and Cryptography Nicolas Sklavos, Xinmiao Zhang, 2017-12-19 As the use of wireless devices becomes widespread so does the need for strong and secure transport protocols Even with this intensified need for securing systems using cryptography does

not seem to be a viable solution due to difficulties in implementation. The security layers of many wireless protocols use outdated encryption algorithms which have proven unsuitable for hardware usage particularly with handheld devices.

Summarizing key issues involved in achieving desirable performance in security implementations Wireless Security and Cryptography Specifications and Implementations focuses on alternative integration approaches for wireless communication security. It gives an overview of the current security layer of wireless protocols and presents the performance characteristics of implementations in both software and hardware. This resource also presents efficient and novel methods to execute security schemes in wireless protocols with high performance. It provides the state of the art research trends in implementations of wireless protocol security for current and future wireless communications. Unique in its coverage of specification and implementation concerns that include hardware design techniques, Wireless Security and Cryptography Specifications and Implementations provides thorough coverage of wireless network security and recent research directions in the field.

Hardware Acceleration of EDA Algorithms Sunil P Khatri, Kanupriya Gulati, 2010-03-11 Single threaded software applications have ceased to see significant gains in performance on a general purpose CPU even with further scaling in very large scale integration VLSI technology. This is a significant problem for electronic design automation (EDA) applications since the design complexity of VLSI integrated circuits (ICs) is continuously growing. In this research monograph we evaluate custom ICs, old programmable gate arrays (FPGAs) and graphics processors as platforms for accelerating EDA algorithms instead of the general purpose single threaded CPU. We study applications which are used in key time consuming steps of the VLSI design flow. Further these applications also have different degrees of inherent parallelism in them. We study both control dominated EDA applications and control plus data parallel EDA applications. We accelerate these applications on these different hardware platforms. We also present an automated approach for accelerating certain uniprocessor applications on a graphics processor. This monograph compares custom ICs, FPGAs and graphics processing units (GPUs) as potential platforms to accelerate EDA algorithms. It also provides details of the programming model used for interfacing with the GPUs.

Low-Energy FPGAs — Architecture and Design Varghese George, Jan M. Rabaey, 2012-12-06 Low Energy FPGAs Architecture and Design is a primary resource for both researchers and practicing engineers in the field of digital circuit design. The book addresses the energy consumption of Field Programmable Gate Arrays (FPGAs). FPGAs are becoming popular as embedded components in computing platforms. The programmability of the FPGA can be used to customize implementations of functions on an application basis. This leads to performance gains and enables reuse of expensive silicon. Chapter 1 provides an overview of digital circuit design and FPGAs. Chapter 2 looks at the implication of deep submicron technology on FPGA power dissipation. Chapter 3 describes the exploration environment to guide and evaluate design decisions. Chapter 4 discusses the architectural optimization process to evaluate the trade offs between the flexibility of the architecture and the effect on the performance metrics. Chapter 5 reviews different circuit techniques to reduce the

performance overhead of some of the dominant components Chapter 6 shows methods to configure FPGAs to minimize the programming overhead Chapter 7 addresses the physical realization of some of the critical components and the final implementation of a specific low energy FPGA Chapter 8 compares the prototype array to an equivalent commercial architecture

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