

# VLSI Physical Design

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Saturday, 20 February 2016

## STA Interview Questions Part 1

What is slack?

What is SDC constraint file contains?

Delay of a cell depends on which factors?

Write Setup and Hold equations?

Where do you get the WDL's? Do you create WDL's? How do you specify?

In which case inserting a buffer will solve the setup timing?

What is cross talk? How it affects timing.

How can you avoid cross talk?

What is shielding? how does it prevents cross talk?

How spacing helps in reducing crosstalk noise?

How buffer can be used in victim to avoid crosstalk?

What are the problems faced related to timing?

How did you resolve the setup and hold problem?

How does delays varies with different PVT conditions? please explain with the help of graph.

What is cell delay and net delay?

What are different delay models available and what are the difference between them?

What is cloning and buffering?

What is the derate value that can be used?

What are the corners you check for timing sign-off? Is there any changes in the derate value for each corner?

Where do you mean by the de-rating value? What are the factors that decide the de-rating values? factor?

What factors decides the setup time of flip-flop?

What is metastability?

In a system with insufficient hold time, will slowing down the clock frequency help?

Posted by Akshay at 22:52

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**Didier Musso**



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perspective Both are important skill sets that all RTL design engineers should have some basic understanding In addition we share a few Behavioral Questions and Useful Interview Tips at the end of this book We do hope you find the information in this book useful for preparing digital design interviews and landing a dream job in the industry      **Gateway to VLSI** Bharat Agarwal, Kshitij Goel,2019-10-04 If you can spare half an hour then we can guarantee success at your next VLSI Very Large Scale Integration FPGA Field Programmable Gate Array STA Static Timing analysis interview Do you want to secure at least 3 to 4 job offers by succeeding at all the phone and on site job interviews for the FPGA DESIGN ENGINEER position Or do you simply want answers for the most frequently asked interview questions in VLSI FPGA digital circuit design Did you know that people who target question answer type preparation for a job interview are 3 4 times more likely to get a job offer than those who don t Did you also know that there is a set of questions that is likely to be repeatedly asked by interviewers across the industry no matter who you talk with in the VLSI FPGA digital design After a total of 17 unsuccessful interviews we thought of writing a book to help upcoming undergrads and experience professionals to get selected in such interviews The book covers every dimension related to FPGA Verilog STA and Protocols In simple words don t search anything on the internet this book is the Google of FPGA and Verilog      Proceedings of the 2007 International Symposium on Physical Design Patrick H. Madden,2007

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