

8. Design of Latches and flip flops: D-latch SR, D,JK, T

Aim: Design of Latches and flip flops (D-latch SR, D,JK, T) using Verilog and simulates the design

Apparatus required: - **Electronics Design Automation Tools used:** -

- Xilinx Spartan 3 FPGA
- Xilinx ISE Simulator tool
- Xilinx XST Synthesis tool
- Xilinx Project Navigator 8.1i
- JTAG cable
- Adaptor 5v/4A

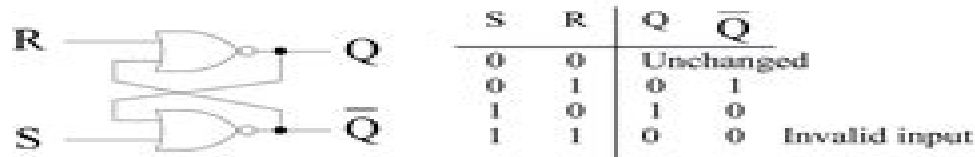
Theory:

LATCH AND FLIP-FLOP

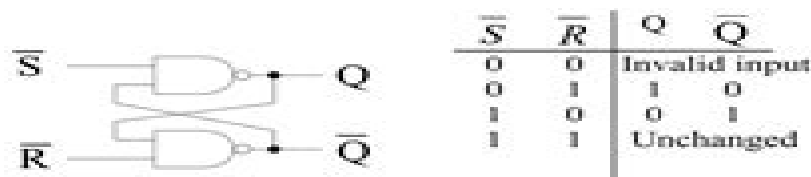
Latch and flip-flop are memory devices and implemented using bistable circuit - its output will remain in either 0 or 1 state. The output state of a latch is controlled by its excitation input signals. A flip-flop (FF) is predominately controlled by a clock and its output state is determined by its excitation input signals. Note that if the clock is replaced by a gated control signal, the flip-flop becomes a gated latch.

a. RS (reset-set) latch circuit

When S (set) is set to 1, the output Q will be set to 1. Likewise, when R (reset) is set to 1, the output Q will be set to 0. It is invalid to set both S and R to 1.



NOR gate implementation



NAND gate implementation

Note that the input is active high for NOR gate implementation, whereas the input is active low for NAND gate implementation.

b. Clocked RS FF

Verilog Manual

**Jean-Michel Bergé, Alain
Fonkoua, Serge Maginot, Jacques
Rouillard**



Verilog Manual:

The Verilog PLI Handbook Stuart Sutherland, 2013-04-18 The Verilog Programming Language Interface commonly called the Verilog PU is one of the more powerful features of Verilog The PU provides a means for both hardware designers and software engineers to interface their own programs to commercial Verilog simulators Through this interface a Verilog simulator can be customized to perform virtually any engineering task desired Just a few of the common uses of the PU include interfacing Verilog simulations to C language models adding custom graphical tools to a simulator reading and writing proprietary file formats from within a simulation performing test coverage analysis during simulation and so forth The applications possible with the Verilog PLI are endless Intended audience this book is written for digital design engineers with a background in the Verilog Hardware Description Language and a fundamental knowledge of the C programming language It is expected that the reader has a basic knowledge of hardware engineering specifically digital design of ASIC and FPGA technologies Is familiar with the Verilog Hardware Description Language HDL and can write models of hardware circuits in Verilog can write simulation test fixtures in Verilog and can run at least one Verilog logic simulator Knows basic C language programming including the use of functions pointers structures and file I/O Explanations of the concepts and terminology of digital *SystemVerilog for Design Second Edition* Stuart Sutherland, Simon Davidmann, Peter Flake, 2006-09-15 SystemVerilog is a rich set of extensions to the IEEE 1364 2001 Verilog Hardware Description Language Verilog HDL These extensions address two major aspects of HDL based design First modeling very large designs with concise accurate and intuitive code Second writing high level test programs to efficiently and effectively verify these large designs The first edition of this book addressed the first aspect of the SystemVerilog extensions to Verilog Important modeling features were presented such as two state data types enumerated types user defined types structures unions and interfaces Emphasis was placed on the proper usage of these enhancements for simulation and synthesis SystemVerilog for Design Second Edition has been extensively revised on a chapter by chapter basis to include the many text and example updates needed to reflect changes that were made between the first edition of this book was written and the finalization of the new standard It is important that the book reflect these syntax and semantic changes to the SystemVerilog language In addition the second edition features a new chapter that explains the SystemVerilog packages a new appendix that summarizes the synthesis guidelines presented throughout the book and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys Mentor and Cadence tools **Digital System Design and Verification Using System Verilog** Mr. Rohit Manglik, 2024-03-06 EduGorilla Publication is a trusted name in the education sector committed to empowering learners with high quality study materials and resources Specializing in competitive exams and academic support EduGorilla provides comprehensive and well structured content tailored to meet the needs of students across various streams and levels *Reuse Techniques for VLSI Design* Ralf Seepold, Arno Kunzmann, 1999-03-31 Reuse

Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design Verilog IEEE Standards Department,1995

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Bricaud, 1998 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available Design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process Proceedings of the ... IEEE International Caracas Conference on Devices, Circuits and Systems, 2000

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