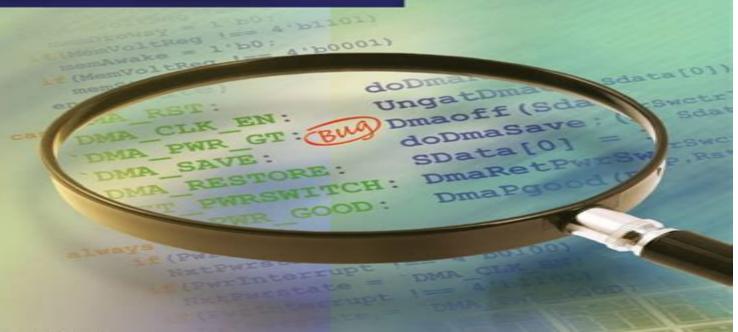
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Daniel Große, Sara Vinco, Hiren Patel

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Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Jose L. Ayala, Braulio Garcia-Camara, Manuel Prieto, Martino Ruggiero, Gilles Sicard, 2011-09-15 This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design PATMOS 2011 held in Madrid Spain in September 2011 The 34 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization *Languages, Design* Methods, and Tools for Electronic System Design* Daniel Große, Sara Vinco, Hiren Patel, 2018-12-19 This book brings together a selection of the best papers from the twentiethedition of the Forum on specification and Design Languages Conference FDL which took place on September 18 20 2017 in Verona Italy FDL is a well established international forum devoted to dissemination of research results practical experiences and new ideas in the application of specification design and verification languages to the design modeling and verification of integrated circuits complex hardware software embedded systems and mixed technology systems Covers modeling and verification methodologies targeting digital and analog systems Addresses firmware development and validation Targets both functional and non functional properties Includes descriptions

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architecture and debugging and test <u>EDN</u>,2000 **Proceedings**,1998 **ASIC & EDA**,1994 **Verification Methodology Manual for SystemVerilog** Janick Bergeron,Eduard Cerny,Alan Hunter,Andy Nightingale,2005-09-28 Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly Unique in its broad coverage of SystemVerilog advanced functional verification and the combination of the two <u>Digest of Papers - Compcon</u>,1997

A Directory of Computer Software Applications ,1979 International Workshop on Memory Technology, **Design, and Testing** Fabrizio Lombardi, Rochit Rajsuman, Thomas Wik, 2001 Annotation The 14 papers in this collection from the August 2001 workshop are divided into five sessions on semiconductor memory design BIST redundancy and error control fault models and multi port SRAM testing and verification and testing Some of the topics are evaluation of redundancy analysis algorithms a parallel approach for testing multi port static random access memories a low output resistance charge pump for flash memory programming BIST based bitfail mapping of an embedded DRAM and an orthogonal transpose RAM cell array architecture with an alternate bit line to bit line contact scheme No subject index c Book News Inc Electronic Design, <u>International Atomic Energy Agency Publications: Catalogue</u> International Atomic **Proceedings** IEEE computer society, Association for computing machinery. Special interest group Energy Agency, 1986 IAEA Nuclear Science Publications, Catalogue International Atomic Energy on microprogramming, 1983 Proceedings VHDL International. Users Forum. Fall Workshop, 1999 Agency, 1980 NASA SP. ,1962

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