

VLSI Fault Modeling and Testing Techniques

**edited by
George W. Zobrist**

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N. K. Jha,S. Gupta



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VLSI Fault Modeling and Testing Techniques George W. Zobrist, 1993 VLSI systems are becoming very complex and difficult to test Traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated circuit Hierarchical models are needed that are easy to use at the transistor and functional levels Stuck open faults present severe testing problems in CMOS circuits to overcome testing problems testable designs are utilized Bridging faults are important due to the shrinking geometry of ICs BIST PLA schemes have common features controllability and observability which are enhanced through additional logic and test points Certain circuit topologies are more easily testable than others The amount of reconvergent fan out is a critical factor in determining realistic measures for determining test generation difficulty Test implementation is usually left until after the VLSI data path has been synthesized into a structural description This leads to investigation methodologies for performing design synthesis with test incorporation These topics and more are discussed

Delay Fault Testing for VLSI Circuits Angela Krstic, Kwang-Ting (Tim) Cheng, 1998-10-31 With the ever increasing speed of integrated circuits violations of the performance specifications are becoming a major factor affecting the product quality level The need for testing timing defects is further expected to grow with the current design trend of moving towards deep submicron devices After a long period of prevailing belief that high stuck at fault coverage is sufficient to guarantee high quality of shipped products the industry is now forced to rethink other types of testing Delay testing has been a topic of extensive research both in industry and in academia for more than a decade As a result several delay fault models and numerous testing methodologies have been proposed Delay Fault Testing for VLSI Circuits presents a selection of existing delay testing research results It combines introductory material with state of the art techniques that address some of the current problems in delay testing Delay Fault Testing for VLSI Circuits covers some basic topics such as fault modeling and test application schemes for detecting delay defects It also presents summaries and conclusions of several recent case studies and experiments related to delay testing A selection of delay testing issues and test techniques such as delay fault simulation test generation design for testability and synthesis for testability are also covered Delay Fault Testing for VLSI Circuits is intended for use by CAD and test engineers researchers tool developers and graduate students It requires a basic background in digital testing The book can be used as supplementary material for a graduate level course on VLSI testing

Register-transfer Level Fault Modeling and Test Evaluation Technique for VLSI Circuits Pradipkumar Arunbhai Thaker, 2000 *Test Generation of Crosstalk Delay Faults in VLSI Circuits* S. Jayanthi, M.C. Bhuvaneshwari, 2018-09-20 This book describes a variety of test generation algorithms for testing crosstalk delay faults in VLSI circuits It introduces readers to the various crosstalk effects and describes both deterministic and simulation based methods for testing crosstalk delay faults The book begins with a focus on currently available crosstalk delay models test generation algorithms for delay faults and crosstalk delay faults before moving on to deterministic algorithms and simulation based algorithms used to test

crosstalk delay faults Given its depth of coverage the book will be of interest to design engineers and researchers in the field of VLSI Testing *Advanced Simulation and Test Methodologies for VLSI Design* G. Russell,I.L. Sayers,1989-02-28

Introduction to Microelectronics to Nanoelectronics Manoj Kumar Majumder,Vijay Rao Kumbhare,Aditya Japa,Brajesh Kumar Kaushik,2020-11-24 Focussing on micro and nanoelectronics design and technology this book provides thorough analysis and demonstration starting from semiconductor devices to VLSI fabrication designing analog and digital on chip interconnect modeling culminating with emerging non silicon nano devices It gives detailed description of both theoretical as well as industry standard HSPICE Verilog Cadence simulation based real time modeling approach with focus on fabrication of bulk and nano devices Each chapter of this proposed title starts with a brief introduction of the presented topic and ends with a summary indicating the futuristic aspect including practice questions Aimed at researchers and senior undergraduate graduate students in electrical and electronics engineering microelectronics nanoelectronics and nanotechnology this book Provides broad and comprehensive coverage from Microelectronics to Nanoelectronics including design in analog and digital electronics Includes HDL and VLSI design going into the nanoelectronics arena Discusses devices circuit analysis design methodology and real time simulation based on industry standard HSPICE tool Explores emerging devices such as FinFETs Tunnel FETs TFETs and CNTFETs including their circuit co designing Covers real time illustration using industry standard Verilog Cadence and Synopsys simulations **Testing of Digital Systems** N. K. Jha,S. Gupta,2003-05-08 Device testing represents the single largest manufacturing expense in the semiconductor industry costing over 40 billion a year The most comprehensive and wide ranging book of its kind Testing of Digital Systems covers everything you need to know about this vitally important subject Starting right from the basics the authors take the reader through automatic test pattern generation design for testability and built in self test of digital circuits before moving on to more advanced topics such as IDDQ testing functional testing delay fault testing memory testing and fault diagnosis The book includes detailed treatment of the latest techniques including test generation for various fault models discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system on a chip test synthesis Written for students and engineers it is both an excellent senior graduate level textbook and a valuable reference Microfluidic Very Large Scale Integration (VLSI) Paul Pop,Wajid Hassan Minhass,Jan Madsen,2016-02-08 This book presents the state of the art techniques for the modeling simulation testing compilation and physical synthesis of mVLSI biochips The authors describe a top down modeling and synthesis methodology for the mVLSI biochips inspired by microelectronics VLSI methodologies They introduce a modeling framework for the components and the biochip architecture and a high level microfluidic protocol language Coverage includes a topology graph based model for the biochip architecture and a sequencing graph to model for biochemical application showing how the application model can be obtained from the protocol language The techniques described facilitate programmability and automation enabling developers in the emerging large

biochip market

Hierarchical Modeling for VLSI Circuit Testing Debashis Bhattacharya, John P. Hayes, 2012-12-06

Test generation is one of the most difficult tasks facing the designer of complex VLSI based digital systems. Much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology. It has long been recognized that the testing problem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation; however, the development of such methods has proceeded very slowly. To be acceptable, high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods. The fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line SSL fault model which is tightly bound to the gate level of abstraction. This monograph presents a novel approach to solving the foregoing problem. It is based on the systematic use of multibit vectors rather than single bits to represent logic signals including fault signals. A circuit is viewed as a collection of high level components such as adders, multiplexers, and registers interconnected by n bit buses. To match this high level circuit model, we introduce a high level bus fault that in effect replaces a large number of SSL faults and allows them to be tested in parallel. However, by reducing the bus size from n to one, we can obtain the traditional gate level circuit and models.

Architecture Design and Validation Methods Egon

Börger, 2012-12-06. This book grew out of material which was taught at the International Summer School on Architecture Design and Validation Methods held June 23-July 5, 1997, on the Island of Lipari and directed to graduate students and young researchers. Since then, the course notes have been completely elaborated and extended, and additional chapters have been added so that this book offers a comprehensive presentation of the state of the art which leads the reader to the forefront of the current research in the area. The chapters, each of which was written by a group of eminent specialists in the field, are self-contained and can be read independently of each other. They cover the wide range of theoretical and practical methods which are currently used for the specification, design, validation, and verification of hardware/software architectures. Synthesis methods are the subject of the first three chapters. The chapter on Modeling and Synthesis of Behavior Control and Data Flow focusses on techniques above the register transfer level. The chapter on Cell Based Logic Optimizations concentrates on methods that interface logic design with physical design, in particular on techniques for cell library binding, the back end of logic synthesis. The chapter on A Design Flow for Performance Planning presents new paradigms for iteration free synthesis where global wire plans for meeting timing constraints already appear at the conceptual design stage, even before fixing the functionality of the blocks in the plan.

Lecture Notes in Analog Electronics Vančo B. Litovski, 2025-01-17

Prof. Vančo Litovski was born in 1947 in Rakita, South Macedonia, Greece. He graduated from the Faculty of Electronic Engineering in Niš in 1970 and obtained his M.Sc. in 1974 and his Ph.D. in 1977. He was appointed as a teaching assistant at the Faculty of Electronic Engineering in 1970 and became a full professor at the same faculty in 1987. He was elected as a visiting professor

honoris causa at the University of Southampton in 1999 From 1987 until 1990 he was a consultant to the CEO of Ei and was the head of the Chair of Electronics at the Faculty of Electronic Engineering in Ni for 12 years From 2015 to 2017 he was a researcher at the University of Bath He received several awards including from the Faculty of Electronic Engineering Charter in 1980 Charter in 1985 and a Special Recognition in 1995 and the University of Ni Plaque 1985

Scientific and Technical Aerospace Reports, 1994 Lists citations with abstracts for aerospace related reports obtained from world wide sources and announces documents that have recently been entered into the NASA Scientific and Technical Information Database

Models in Hardware Testing Hans-Joachim Wunderlich, 2009-11-12 Model based testing is the most powerful technique for testing hardware and software systems Models in Hardware Testing describes the use of models at all the levels of hardware testing The relevant fault models for nanoscaled CMOS technology are introduced and their implications on fault simulation automatic test pattern generation fault diagnosis memory testing and power aware testing are discussed Models and the corresponding algorithms are considered with respect to the most recent state of the art and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance

The Electronics Handbook Jerry C. Whitaker, 2018-10-03 During the ten years since the appearance of the groundbreaking bestselling first edition of The Electronics Handbook the field has grown and changed tremendously With a focus on fundamental theory and practical applications the first edition guided novice and veteran engineers along the cutting edge in the design production installation operation and maintenance of electronic devices and systems Completely updated and expanded to reflect recent advances this second edition continues the tradition The Electronics Handbook Second Edition provides a comprehensive reference to the key concepts models and equations necessary to analyze design and predict the behavior of complex electrical devices circuits instruments and systems With 23 sections that encompass the entire electronics field from classical devices and circuits to emerging technologies and applications The Electronics Handbook Second Edition not only covers the engineering aspects but also includes sections on reliability safety and engineering management The book features an individual table of contents at the beginning of each chapter which enables engineers from industry government and academia to navigate easily to the vital information they need This is truly the most comprehensive easy to use reference on electronics available

Machine Learning and Intelligent Communications Xuemai Gu, Gongliang Liu, Bo Li, 2018-01-20 This two volume set constitutes the refereed post conference proceedings of the Second International Conference on Machine Learning and Intelligent Communications MLICOM 2017 held in Weihai China in August 2017 The 143 revised full papers were carefully selected from 225 submissions The papers are organized thematically in machine learning intelligent positioning and navigation intelligent multimedia processing and security intelligent wireless mobile network and security cognitive radio and intelligent networking intelligent internet of things intelligent satellite communications and networking intelligent remote sensing visual computing and three dimensional modeling green communication and intelligent

networking intelligent ad hoc and sensor networks intelligent resource allocation in wireless and cloud networks intelligent signal processing in wireless and optical communications intelligent radar signal processing intelligent cooperative communications and networking

System-on-Chip Test Architectures Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, 2010-07-28 Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs. Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations, examples. Most up to date coverage available including Fault Tolerance, Low Power Testing, Defect and Error Tolerance, Network on Chip, NOC Testing, Software Based Self Testing, FPGA Testing, MEMS Testing, and System In Package, SIP Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era, promising nanotechnology test techniques including Quantum Dots, Cellular Automata, Carbon Nanotubes, and Hybrid Semiconductor Nanowire Molecular Computing. Practical problems at the end of each chapter for students.

Digital Circuit Testing and Testability Parag K. Lala, 1997 An easy to use introduction to the practices and techniques in the field of digital circuit testing. Lala writes in a user friendly and tutorial style, making the book easy to read even for the newcomer to fault tolerant system design. Each informative chapter is self contained with little or no previous knowledge of a topic assumed. Extensive references follow each chapter.

Economics of Electronic Design, Manufacture and Test M. Abadir, T. Ambler, 2013-06-29 The general understanding of design is that it should lead to a manufacturable product. Neither the design nor the process of manufacturing is perfect. As a result, the product will be faulty and will require testing and fixing. Where does economics enter this scenario? Consider the cost of testing and fixing the product. If a manufactured product is grossly faulty or too many of the products are faulty, the cost of testing and fixing will be high. Suppose we do not like that. We then ask what is the cause of the faulty product. There must be something wrong in the manufacturing process. We trace this cause and fix it. Suppose we fix all possible causes and have no defective products. We would have eliminated the need for testing. Unfortunately, things are not so perfect. There is a cost involved with finding and eliminating the causes of faults. We thus have two costs: the cost of testing and fixing, we will call it cost 1, and the cost of finding and eliminating causes of faults, call it cost 2. Both costs in some way are included in the overall cost of the product. If we try to eliminate cost 1, cost 2 goes up and vice versa. An economic system of production will minimize the overall cost of

the product Economics of Electronic Design Manufacture and Test is a collection of research contributions derived from the Second Workshop on Economics of Design Manufacture and Test written for inclusion in this book

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Manoj Sachdev, José Pineda de Gyvez, 2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC VLSI circuits testing is an activity associated with every level of integration However special emphasis is placed for wafer level test and final test Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted Basic digital tests are applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing DDQ stuck at testing low voltage testing etc This partitioning choice is actually application dependent

Integrated Circuit Test Engineering Ian A. Grout, 2005-08-22 Using the book and the software provided with it the reader can build his her own tester arrangement to investigate key aspects of analog digital and mixed system circuits Plan of attack based on traditional testing circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

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