VHDL

Answers to Frequently Asked Questions Second Edition



Ben Cohen



Vhdl Answers To Frequently Asked Questions

Peter J. Ashenden, Gregory D. Peterson, Darrell A. Teegarden

Vhdl Answers To Frequently Asked Questions:

VHDL Answers to Frequently Asked Questions Ben Cohen,1998-01-31 VHDL Answers to Frequently asked Questions is a follow up to the author's book VHDL Coding Styles and Methodologies ISBN 0 7923 9598 0 On completion of his first book the author continued teaching VHDL and actively participated in the comp lang vhdl newsgroup During his experiences he was enlightened by the many interesting issues and questions relating to VHDL and synthesis These pertained to misinterpretations in the use of the language methods for writing error free and simulation efficient code for testbench designs and for synthesis and general principles and guidelines for design verification As a result of this wealth of public knowledge contributed by a large VHDL community the author decided to act as a facilitator of this information by collecting different classes of VHDL issues and by elaborating on these topics through complete simulatable examples Titis book is intended for those who are seeking an enhanced proficiency in VHDL Its target audience includes 1 Engineers The book addresses a set of problems commonly experienced by real users of VHDL It provides practical explanations to the questions and suggests practical solutions to the raised issues It also includes packages of common utilities that are useful in the generation of debug code and testbench designs These packages include conversions to strings the IMAGE package generation of Linear Feedback Shift Registers LFSR Multiple Input Shift Register MISR and random number generators

VHDL Answers to Frequently Asked Questions Ben Cohen, 2013-03-09 VHDL Answers to Frequently asked Questions is a follow up to the author s book VHDL Coding Styles and Methodologies ISBN 0 7923 9598 0 On completion of his first book the author continued teaching VHDL and actively participated in the comp lang vhdl newsgroup During his experiences he was enlightened by the many interesting issues and questions relating to VHDL and synthesis These pertained to misinterpretations in the use of the language methods for writing error free and simulation efficient code for testbench designs and for synthesis and general principles and guidelines for design verification As a result of this wealth of public knowledge contributed by a large VHDL community the author decided to act as a facilitator of this information by collecting different classes of VHDL issues and by elaborating on these topics through complete simulatable examples This book is intended for those who are seeking an enhanced proficiency in VHDL Its target audience includes 1 Engineers The book addresses a set of problems commonly experienced by real users of VHDL It provides practical explanations to the questions and suggests practical solutions to the raised issues It also includes packages to achieve common utilities useful in the generation of debug code aDd testbench designs These packages include conversions to strings the IMAGE package generation of Linear Feedback Shift Registers LFSR Multiple Input Shift Register MISR and random number generators

Vhdl Answers To Frequently Asked Questions, 2E Cohen,2007-11-01 Real Chip Design and Verification Using Verilog and VHDL Ben Cohen,2002 This book concentrates on common classes of hardware architectures and design problems and focuses on the process of transitioning design requirements into synthesizable HDL code Using his extensive

wide ranging experience in computer architecture and hardware design as well as in his training and consulting work Ben provides numerous examples of real life designs illustrated with VHDL and Verilog code This code is shown in a way that makes it easy for the reader to gain a greater understanding of the languages and how they compare All code presented in the book is included on the companion CD along with other information such as application notes The SGML FAO Book S.J. DeRose, 2007-12-23 Although not evident to all many people have been waiting more than a decade for The SGML FAQ Book by Steve DeRose It has been brewing for a long time with many hours months years of research talking to people gathering their ideas listening to their frustrations applauding their successes Only Steve with his experience credentials wit and enthusiasm for the subject could have written this book But it is also a measure of the success and maturity of ISO 8879 and its amazing longevity that allows an SGMLer to write such a book We can now laugh at ourselves even disclose our mistakes without fear of the other guy While most would not recognize it the revolution known as the World Wide Web would not have happened without a non proprietary easy and almost portable way to create and distribute documents across a widely disparate set of computers networks even countries HTML an SGML application enabled this and as a result the world and the SGML community will never be the same For some the term SGML means order management standards discipline to others the term brings images of pain confusion complexity and pitfalls To all who have engaged in it the Standard means hard work good friends savings in terms of time money and effort a sense of accomplishment and best of all fun This book adds immeasurably to all of these Enjoy the quote from Through Looking by Lewis Carroll as much as we have Coding Styles and Methodologies Ben Cohen, 2007-05-08 VHDL Coding Styles and Methodologies Edition is a follow up book to the first edition of same book and to VHDL Answers to Frequently Asked Questions first and second editions This book was originally written as a teaching tool for a VHDL training course The author began writing the book because he could not find a practical and easy to read book that gave in depth coverage of both the language and coding methodologies This edition provides practical information on reusable software methodologies for the design of bus functional models for testbenches It also provides guidelines in the use of VHDL for synthesis All VHDL code described in the book is on a companion CD The CD also includes the GNU toolsuite with EMACS language sensitive editor with VHDL Verilog and other language templates and TSHELL tools that emulate a Unix shell Model Technology graciously included a timed evaluation version of ModelSim a recognized industry standard VHDL Verilog compiler and simulator that supports easy viewing of the models under analysis along with many debug features In addition Synplicity included a timed version of Synplify a very efficient user friendly and easy to use FPGA synthesis tool Synplify provides a user both the RTL and gate level views of the synthesized model and a performance report of the design Optimization mechanisms are provided in the tool Digital Integrated Circuit Design Hubert Kaeslin, 2008-04-28 This practical tool independent guide to designing digital circuits takes a unique top down approach reflecting the nature of the design process in industry Starting with architecture design the book comprehensively

explains the why and how of digital circuit design using the physics designers need to know and no more **SystemVerilog** Assertions Handbook Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, 2005 Component Design by Example Ben Using PSL/Sugar for Formal and Dynamic Verification Ben Cohen, Srinivasan Venkataramanan, Ajeetha Cohen, 2001 Writing Testbenches Janick Bergeron, 2007-05-08 CHAPTER 6 Architecting Testbenches 221 Reusable Kumari,2004 Verification Components 221 Procedural Interface 225 Development Process 226 Verilog Implementation 227 Packaging Bus Functional Models 228 Utility Packages 231 VHDL Implementation 237 Packaging Bus Functional Procedures 238 240 Creating a Test Harness 243 Abstracting the Client Server Protocol Managing Control Signals 246 Multiple Server Instances 247 Utility Packages 249 Autonomous Generation and Monitoring 250 Autonomous Stimulus 250 Random Stimulus 253 Injecting Errors 255 Autonomous Monitoring 255 258 Autonomous Error Detection Input and Output Paths 258 Programmable Testbenches 259 Configuration Files 260 Concurrent Simulations 261 Compile Time Configuration 262 Verifying Configurable Designs 263 Configurable Testbenches 265 Top Level Generics and Parameters 266 Summary 268 CHAPTER 7 Simulation Management 269 Behavioral Models 269 Behavioral versus Synthesizable Models 270 Example of Behavioral Modeling 271 Characteristics of a Behavioral Model 273 x Writing Testbenches Functional Verification of HDL Models Modeling Reset 276 Writing Good Behavioral Models 281 Behavioral Models Are Faster 285 The Cost of Behavioral Models 286 The Benefits of Behavioral Models 286 Demonstrating Equivalence 289 Pass or Fail 289 Managing Simulations 292 294 Configuration Management Verilog Configuration Management 295 VHDL Configuration Management 301 SDF Back Annotation 305 Output File Management 309 Regression 312 Running Regressions 313 Regression Management 314 Summary 316 APPENDIX A Coding Guidelines 317 Directory Structure 318 VHDL Specific 320 Verilog Specific 320 General Coding Guidelines 321 Comments 321 Layout 323 Syntax 326 Debugging 329 Naming Guidelines 329 Capitalization 330 Identifiers 332 Constants 334 334 HDL SpecificFilenames 336 HDL Coding Guidelines 336 337 Structure 337 Layout

The Student's Guide to VHDL Peter J. Ashenden, 2008-05-19 The Student's Guide to VHDL is a condensed edition of The Designer's Guide to VHDL the most widely used textbook on VHDL for digital system modeling The Student's Guide is targeted as a supplemental reference book for computer organization and digital design courses Since publication of the first edition of The Student's Guide the IEEE VHDL and related standards have been revised The Designer's Guide has been revised to reflect the changes so it is appropriate that The Student's Guide also be revised In The Student's Guide to VHDL 2nd Edition we have included a design case study illustrating an FPGA based design flow The aim is to show how VHDL modeling fits into a design flow starting from high level design and proceeding through detailed design and verification synthesis FPGA place and route and final timing verification Inclusion of the case study helps to better serve the educational market Currently most college courses do not formally address the details of design flow Students may be given informal guidance on how to proceed with lab projects In many cases it is left to students to work it out for themselves The case study

in The Student's Guide provides a reference design flow that can be adapted to a variety of lab projects The System Designer's Guide to VHDL-AMS Peter J. Ashenden, Gregory D. Peterson, Darrell A. Teegarden, 2002-09-10 The demand is exploding for complete integrated systems that sense process manipulate and control complex entities such as sound images text motion and environmental conditions These systems from hand held devices to automotive sub systems to aerospace vehicles employ electronics to manage and adapt to a world that is predominantly neither digital nor electronic To respond to this design challenge the industry has developed and standardized VHDL AMS a unified design language for modeling digital analog mixed signal and mixed technology systems VHDL AMS extends VHDL to bring the successful HDL modeling methodology of digital electronic systems design to these new design disciplines Gregory Peterson and Darrell Teegarden join best selling author Peter Ashenden in teaching designers how to use VHDL AMS to model these complex systems This comprehensive tutorial and reference provides detailed descriptions of both the syntax and semantics of the language and of successful modeling techniques It assumes no previous knowledge of VHDL but instead teaches VHDL and VHDL AMS in an integrated fashion just as it would be used by designers of these complex integrated systems Explores the design of an electric powered unmanned aerial vehicle system UAV in five separate case studies to illustrate mixed signal mixed technology power systems communication systems and full system modeling **Writing Testbenches: Functional Verification of HDL Models** Janick Bergeron, 2012-12-06 mental improvements during the same period What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough In the second edition of Writing Testbenches Bergeron raises the verification level of abstraction by introducing coverage driven constrained random transaction level self checking testbenches all made possible through the introduction of hardware verification languages HVLs such as e from Verisity and OpenVera from Synopsys The state of art methodologies described in Writing Test benches will contribute greatly to the much needed equivalent of a synthesis breakthrough in verification productivity I not only highly recommend this book but also I think it should be required reading by anyone involved in design and verification of today's ASIC SoCs and systems Harry Foster Chief Architect Verplex Systems Inc xviii Writing Testbenches Functional Verification of HDL Models PREFACE If you survey hardware design groups you will learn that between 60% and 80% of their effort is now dedicated to verification CPU Design Chandra Thimmannagari, 2005-12-02 I am honored to write the foreword for Chandra Thimmannagari s book on CPU design Chandra s book provides a practical overview of Microprocessor and high end ASIC design as practiced today It is a valuable addition to the literature on CPU design and is made possible by Chandra's unique combination of extensive hands on CPU design experience at companies such as AMD and Sun Microsystems and a passion for writing Technical books related to CPU design are almost always written by researchers in academia or industry and tend to pick one area CPU architecture Bus architecture CMOS design that is the area of expertise of the author and present that in great detail Suchbooks are of great value to students and

practitioners in that area However engineers working on CPU design need to develop an understanding of areas outside their own to be effective CPU design is a multi dimensional problem and one dimensional optimization is often counterproductive

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