EXPERIEMENT NO. 2

Simulation using all the modeling styles and Synthesis of 1-bit half adder and 1-bit Full adder using verilog HDL

AIME:

Perform Zero Delay Simulation of 1-bit half adder and 1-bit Full adder written in behavioral, dataflow and structural modeling style in VERILOG HDL using a Test bench. Then, Synthesize each one of them on two different EDA tools.

Electronics Design Automation Tools used:

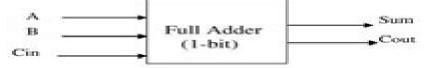
- i) FPGA Advantage 3.1 (includes Model Sim simulation tool and Leonardo Spectrum Synthesis Tool)
- ii) Xilinx Project Navigator 8.1 (Includes all the steps in the design flow from Simulation to Implementation to download onto FPGA).

Block Diagram:

1-bit Half Adder:



1-bit Full Adder:



Truth table:

Half Adder:

A	В	Sum	Carry	
0	0	0	0	
O	1	1	O	
1	0	1	0	
1	1	0	1	

Rivelli A elelence

E MILL /SAPAGET :					
A	13	Cin	Sum	Court	

Vhdl Lab Manual Question And Ans

Milos D. Ercegovac, Tom?s Lang, Jaime H. Moreno

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Questions, 2E Cohen, 2007-11-01 VHDL Designer's Reference Jean-Michel Bergé, Alain Fonkoua, Serge Maginot, Jacques Rouillard, 1992-05-31 too vast too complex too grand for description John Wesley Powell 1870 discovering the Grand Canyon VHDL is a big world A beginner can be easily disappointed by the generality of this language This generality is explained by the large number of domains covered from specifications to logical simulation or synthesis To the very beginner VHDL appears as a kit He is quickly aware that his problem may be solved with VHDL but does not know how He does not even know how to start In this state of mind all the constraints that can be set to his modeling job by using a subset of the language or a given design methodology may be seen as a life preserver. The success of the introduction of VHDL in a company depends on solutions to many questions that should be answered months before the first line of code is written Why choose VHDL Which VHDL tools should be chosen Which modeling methodology should be adopted How should the VHDL environment be customized What are the tricks Where are the traps What are the differences between VHDL and other competing HDLs Answers to these questions are organized according to different concerns buying the tools organizing the environment and designing Decisions taken in each of these areas may have many consequences on the way to the acceptance and efficiently use of VHDL in a company Digital Logic Simulation and CPLD Programming with VHDL Steve Waterman, 2003 For freshman level courses in Introduction to Digital Electronics sophomore level courses in Introduction to Microprocessors and other middle upper level courses in Digital Electronics This lab manual written around software and hardware developments of the past ten years focuses on the fundamentals of digital electronics and use of Max Plus II software by Altera Corporation Lab sequences start with digital gates and logic control circuits progress to MSI devices latches and flip flops and cover clock dependent circuits and LPM MEGA functions available in the software Introduction to VHDL ,1997 Introduction to VHDL R.D. Hunter, T. T. Johnson, 1996 Covers all aspects of the VHDL language

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