Andrew B. Kahng Jens Lienig Igor L. Markov Jin Hu

VLSI Physical Design: From Graph Partitioning to Timing Closure

Second Edition



Vlsi Physical Design From Graph Partitioning To Timing Closure

Victor Champac, Jose Garcia Gervacio

Vlsi Physical Design From Graph Partitioning To Timing Closure:

VLSI Physical Design: From Graph Partitioning to Timing Closure Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu,2011-01-27 Design and optimization of integrated circuits are essential to the creation of new semiconductor chips and physical optimizations are becoming more prominent as a result of semiconductor scaling Modern chip design has become so complex that it is largely performed by specialized software which is frequently updated to address advances in semiconductor technologies and increased problem complexities A user of such software needs a high level understanding of the underlying mathematical models and algorithms On the other hand a developer of such software must have a keen understanding of computer science aspects including algorithmic performance bottlenecks and how various algorithms operate and interact VLSI Physical Design From Graph Partitioning to Timing Closure introduces and compares algorithms that are used during the physical design phase of integrated circuit design wherein a geometric chip layout is produced starting from an abstract circuit design The emphasis is on essential and fundamental techniques ranging from hypergraph partitioning and circuit placement to timing closure VLSI Physical Design: From Graph Partitioning to Timing Closure Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, 2022-06-14 The complexity of modern chip design requires extensive use of specialized software throughout the process To achieve the best results a user of this software needs a high level understanding of the underlying mathematical models and algorithms In addition a developer of such software must have a keen understanding of relevant computer science aspects including algorithmic performance bottlenecks and how various algorithms operate and interact This book introduces and compares the fundamental algorithms that are used during the IC physical design phase wherein a geometric chip layout is produced starting from an abstract circuit design This updated second edition includes recent advancements in the state of the art of physical design and builds upon foundational coverage of essential and fundamental techniques Numerous examples and tasks with solutions increase the clarity of presentation and facilitate deeper understanding A comprehensive set of slides is available on the Internet for each chapter simplifying use of the book in instructional settings This improved second edition of the book will continue to serve the EDA and design community well It is a foundational text and reference for the next generation of professionals who will be called on to continue the advancement of our chip design tools and design the most advanced micro electronics Dr Leon Stok Vice President Electronic Design Automation IBM Systems Group This is the book I wish I had when I taught EDA in the past and the one I m using from now on Dr Louis K Scheffer Howard Hughes Medical Institute I would happily use this book when teaching Physical Design I know of no other work that s as comprehensive and up to date with algorithmic focus and clear pseudocode for the key algorithms The book is beautifully designed Prof John P Hayes University of Michigan The entire field of electronic design automation owes the authors a great debt for providing a single coherent source on physical design that is clear and tutorial in nature while providing details on key state of the art topics such as timing closure Prof Kurt Keutzer

University of California Berkeley An excellent balance of the basics and more advanced concepts presented by top experts in the field Prof Sachin Sapatnekar University of Minnesota **Graphs in VLSI** Rassul Bairamkulov, Ebv G. Friedman, 2022-11-28 Networks are pervasive Very large scale integrated VLSI systems are no different consisting of dozens of interconnected subsystems hundreds of modules and many billions of transistors and wires Graph theory is crucial for managing and analyzing these systems In this book VLSI system design is discussed from the perspective of graph theory Starting from theoretical foundations the authors uncover the link connecting pure mathematics with practical product development This book not only provides a review of established graph theoretic practices but also discusses the latest advancements in graph theory driving modern VLSI technologies covering a wide range of design issues such as synchronization power network models and analysis and interconnect routing and synthesis Provides a practical introduction to graph theory in the context of VLSI systems engineering Reviews comprehensively graph theoretic methods and algorithms commonly used during VLSI product development process Includes a review of novel graph theoretic methods and algorithms for VLSI system design Algorithm Engineering Lasse Kliemann, Peter Sanders, 2016-11-10 Algorithm Engineering is a methodology for algorithmic research that combines theory with implementation and experimentation in order to obtain better algorithms with high practical impact Traditionally the study of algorithms was dominated by mathematical worst case analysis In Algorithm Engineering algorithms are also implemented and experiments conducted in a systematic way sometimes resembling the experimentation processes known from fields such as biology chemistry or physics This helps in counteracting an otherwise growing gap between theory and practice **Numerical Methods and Applications** Geno Nikolov, Natalia Kolkovska, Krassimir Georgiev, 2019-01-21 This book constitutes the thoroughly refereed post conference proceedings of the 9th International Conference on Numerical Methods and Applications NMA 2018 held in Borovets Bulgaria in August 2018 The 56 revised regular papers presented were carefully reviewed and selected from 61 submissions for inclusion in this book The papers are organized in the following topical sections numerical search and optimization problem driven numerical method motivation and application numerical methods for fractional diffusion problems orthogonal polynomials and numerical quadratures and Monte Carlo and Quasi Monte Carlo methods

<u>Very-Large-Scale Integration Physical Design</u> Kim Ho Yeap, Ing Ming Tan, 2025-01-17 This book presents an innovative approach to rectify Timing Design Rule Check TDRC violations in Very Large Scale Integration VLSI chip design Through the utilization of Tool Command Language TCL scripting this automated solution streamlines the Engineering Change Order ECO process offering efficiency accuracy and accessibility By incorporating various strategies such as cell up sizing low threshold voltage cell swapping and buffer insertion the authors tackle TDRC violations with precision Their methodology integrates a slope violation percentage based guide and net length based buffer insertion strategy tailored to address specific violations effectively Moreover the proactive integration of a Non Linear Delay Model NLDM look up table ensures robust timing

optimization preventing hold timing violations This comprehensive guide navigates fundamental placement rules and ECO implementation featuring a two step approach named make shorts into opens to resolve violations efficiently Impressively the automated TDRC Fixer achieves an 87% TDRC violation fix rate with minimal global timing shifts showcasing the effectiveness of TCL scripting in VLSI physical design workflows This book is a must read for professionals researchers and students seeking to enhance their understanding of VLSI chip design methodologies and optimize their ECO workflows with pragmatic and accessible solutions Algorithmic Aspects in Information and Management Qiufen Ni, Weili Wu,2022-09-18 This book constitutes the proceedings of the 16th International Conference on Algorithmic Aspects in Information and Management AAIM 2022 which was held online during August 13 14 2022 The conference was originally planned to take place in Guangzhou China but changed to a virtual event due to the COVID 19 pandemic The 41 regular papers included in this book were carefully reviewed and selected from 59 submissions **Graph-Theoretic Concepts in Computer Science** Dieter Kratsch, Ioan Todinca, 2014-10-20 This book constitutes the thoroughly refereed post conference proceedings of the 40th International Workshop on Graph Theoretic Concepts in Computer Science WG 2014 held in Nouan le Fuzelier France in June 2014 The 32 revised full papers presented were carefully reviewed and selected from 80 submissions The book also includes two invited papers The papers cover a wide range of topics in graph theory related to computer science such as design and analysis of sequential parallel randomized parameterized and distributed graph and network algorithms structural graph theory with algorithmic or complexity applications computational complexity of graph and network problems graph grammars graph rewriting systems and graph modeling graph drawing and layouts computational geometry random graphs and models of the web and scale free networks and support of these concepts by suitable implementations and applications Timing Performance of Nanometer Digital Circuits Under Process **Variations** Victor Champac, Jose Garcia Gervacio, 2018-04-18 This book discusses the digital design of integrated circuits under process variations with a focus on design time solutions. The authors describe a step by step methodology going from logic gates to logic paths to the circuit level Topics are presented in comprehensively without overwhelming use of analytical formulations Emphasis is placed on providing digital designers with understanding of the sources of process variations their impact on circuit performance and tools for improving their designs to comply with product specifications Various circuit level design hints are highlighted so that readers can use then to improve their designs A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits This book enables readers to make optimal decisions at design time toward more efficient circuits with better yield and higher reliability

<u>Cooperative Game Theory Tools in Coalitional Control Networks</u> Francisco Javier Muros, 2019-04-24 This book analyzes coalitional control schemes by incorporating concepts of cooperative game theory into a distributed control framework It considers a networked architecture where the nodes are the agents and the edges are their communication links and either

the agents or the links are established as the players of cooperative games related to the cost function of the coalitional schemes The book discusses various cooperative game theory tools that are used to measure analyze the players features impose constraints on them provide alternative methods of game computation detect critical players inside the control scheme and perform system partitioning of large scale systems such as the Barcelona drinking water network which is described in a case study

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