

Kazuo Kondo · Masahiro Kado
Kenji Takahashi Editors

Three- Dimensional Integration of Semiconductors

Processing, Materials, and Applications



Springer

Three Dimensional Integration Semiconductors Processing Applications

**Philip Garrou, Christopher Bower, Peter
Ramm**



Three Dimensional Integration Semiconductors Processing Applications:

Three-Dimensional Integration of Semiconductors Kazuo Kondo, Morihiro Kada, Kenji Takahashi, 2015-12-09 This book starts with background concerning three dimensional integration including their low energy consumption and high speed image processing and then proceeds to how to construct them and which materials to use in particular situations The book covers numerous applications including next generation smart phones driving assistance systems capsule endoscopes homing missiles and many others The book concludes with recent progress and developments in three dimensional packaging as well as future prospects

Three-Dimensional Integration of Semiconductors Kazuo Kondo, Morihiro Kada, Kenji Takahashi, 2015 This book starts with background concerning three dimensional integration including their low energy consumption and high speed image processing and then proceeds to how to construct them and which materials to use in particular situations The book covers numerous applications including next generation smart phones driving assistance systems capsule endoscopes homing missiles and many others The book concludes with recent progress and developments in three dimensional packaging as well as future prospects

Handbook of 3D Integration, Volume 1 Philip Garrou, Christopher Bower, Peter Ramm, 2011-09-22 The first encompassing treatise of this new but very important field puts the known physical limitations for classic 2D electronics into perspective with the requirements for further electronics developments and market necessities This two volume handbook presents 3D solutions to the feature density problem addressing all important issues such as wafer processing die bonding packaging technology and thermal aspects It begins with an introductory part which defines necessary goals existing issues and relates 3D integration to the semiconductor roadmap of the industry Before going on to cover processing technology and 3D structure fabrication strategies in detail This is followed by fields of application and a look at the future of 3D integration The contributions come from key players in the field from both academia and industry including such companies as Lincoln Labs Fraunhofer RPI ASET IMEC CEA LETI IBM and Renesas

Wafer Level 3-D ICs Process Technology Chuan Seng Tan, Ronald J. Gutmann, L. Rafael Reif, 2009-06-29 Three dimensional 3D integration is clearly the simplest answer to most of the semiconductor industry's vexing problems heterogeneous integration and reductions of power form factor delay and even cost Conceptually the power latency and form factor of a system with a fixed number of transistors all scale roughly linearly with the diameter of the smallest sphere enclosing frequently interacting devices This clearly provides the fundamental motivation behind 3D technologies which vertically stack several strata of device and interconnect layers with high vertical interconnectivity In addition the ability to vertically stack strata with divergent and even incompatible processes provides for low cost and low parasitic integration of diverse technologies such as sensors energy scavengers nonvolatile memory dense memory fast memory processors and RF layers These capabilities coupled with today's trends of increasing levels of integrated functionality lower power smaller form factor increasingly divergent processes and functional diversification would seem to make 3D technologies a natural choice

for most of the semiconductor industry Since the concept of vertical integration of different strata has been around for over 20 years why aren't vertically stacked strata endemic to the semiconductor industry The simple answer to this question is that in the past the 3D advantages while interesting were not necessary due to the tremendous opportunities offered by geometric scaling In addition even when the global interconnect problem of high performance single core processors seemed insurmountable without innovations such as 3D alternative architectural solutions such as multicores could effectively delay but not eliminate the need for 3D

Handbook of Compound Semiconductors Paul H. Holloway, Gary E. McGuire, 1996-12-31 This book reviews the recent advances and current technologies used to produce microelectronic and optoelectronic devices from compound semiconductors It provides a complete overview of the technologies necessary to grow bulk single crystal substrates grow hetero or homoepitaxial films and process advanced devices such as HBT's QW diode lasers etc

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Semiconductor Wafer Bonding VII : Science, Technology, and Applications, 2003

Three-Dimensional Integrated Circuit Design Yuan Xie, Jingsheng Jason Cong, Sachin Sapatnekar, 2009-12-02 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore's law This observation stated that transistor density in integrated circuits doubles every 1.52 years This came with the simultaneous improvement of individual device performance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore's law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device static currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with multiple cores each running at a few GHz at the most The goal is to continue improving

performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be efficiently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs **Three-Dimensional Design**

Methodologies for Tree-based FPGA Architecture Vinod Pangracious,Zied Marrakchi,Habib Mehrez,2015-06-25 This book focuses on the development of 3D design and implementation methodologies for Tree based FPGA architecture It also stresses the needs for new and augmented 3D CAD tools to support designs such as the design for 3D to manufacture high performance 3D integrated circuits and reconfigurable FPGA based systems This book was written as a text that covers the foundations of 3D integrated system design and FPGA architecture design It was written for the use in an elective or core course at the graduate level in field of Electrical Engineering Computer Engineering and Doctoral Research programs No previous background on 3D integration is required nevertheless fundamental understanding of 2D CMOS VLSI design is required It is assumed that reader has taken the core curriculum in Electrical Engineering or Computer Engineering with courses like CMOS VLSI design Digital System Design and Microelectronics Circuits being the most important It is accessible for self study by both senior students and professionals alike *Handbook of Wafer Bonding* Peter Ramm,James Jian-Qiang Lu,Maaike M. V. Taklo,2012-02-13 The focus behind this book on wafer bonding is the fast paced changes in the research and development in three dimensional 3D integration temporary bonding and micro electro mechanical systems MEMS with new functional layers Written by authors and edited by a team from microsystems companies and industry near research organizations this handbook and reference presents dependable first hand information on bonding technologies Part I sorts the wafer bonding technologies into four categories Adhesive and Anodic Bonding Direct Wafer Bonding Metal Bonding and Hybrid Metal Dielectric Bonding Part II summarizes the key wafer bonding applications developed recently that is 3D integration MEMS and temporary bonding to give readers a taste of the significant applications of wafer bonding technologies This book is aimed at materials scientists semiconductor physicists the semiconductor industry IT engineers electrical engineers and libraries

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