

VLSI Physical Design

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Saturday, 20 February 2016

STA Interview Questions Part 1

What is slack?

What is SDC constraint file contains?

Delay of a cell depends on which factors?

Write Setup and Hold equations?

Where do you get the WDL's? Do you create WDL's? How do you specify?

In which case inserting a buffer will solve the setup timing?

What is cross talk? How it affects timing.

How can you avoid cross talk?

What is shielding? how does it prevents cross talk?

How spacing helps in reducing crosstalk noise?

How buffer can be used in victim to avoid crosstalk?

What are the problems faced related to timing?

How did you resolve the setup and hold problem?

How does delays varies with different PVT conditions? please explain with the help of graph.

What is cell delay and net delay?

What are different delay models available and what are the difference between them?

What is cloning and buffering?

What is the derate value that can be used?

What are the corners you check for timing sign-off? Is there any changes in the derate value for each corner?

Where do you mean by the de-rating value? What are the factors that decide the de-rating values? factor?

What factors decides the setup time of flip-flop?

What is metastability?

In a system with insufficient hold time, will slowing down the clock frequency help?

Posted by Akshay at 22:52

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Design Patrick H. Madden,2007

Proceedings of the 2007 International Symposium on Physical

The Enigmatic Realm of **Vlsi Physical Design Interview Questions**: Unleashing the Language is Inner Magic

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