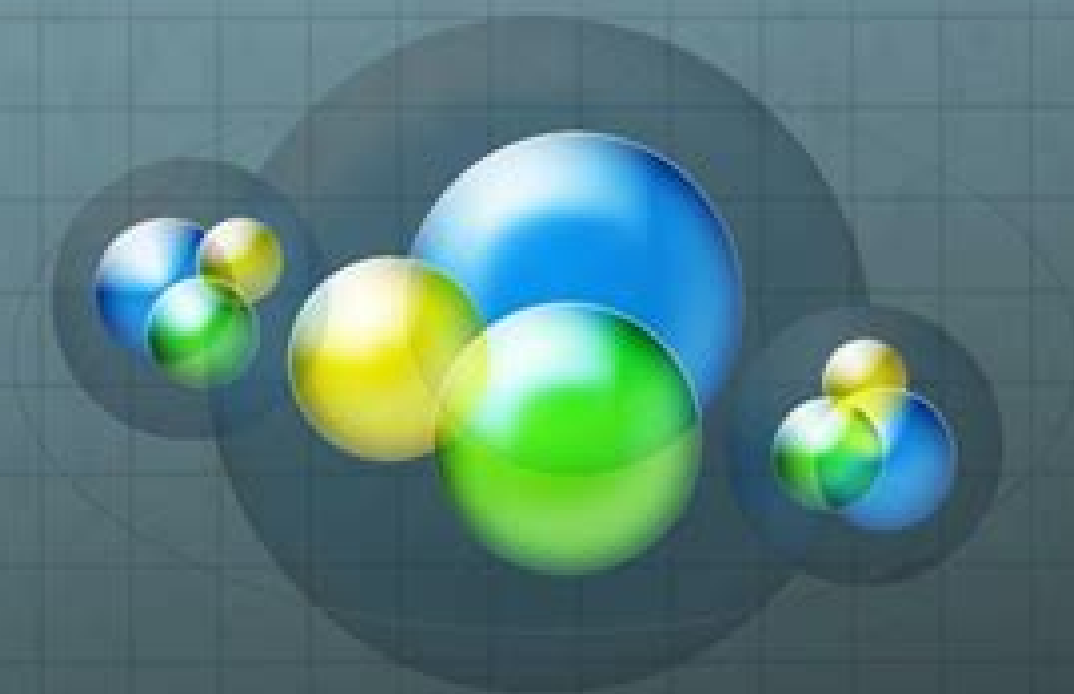




SPIN Verification System

The Model Checker SPIN By Gerard J. Holzmann

Comp 587 – 12/2/09
Eduardo Borjas – Omer Azmon



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The SPIN Verification System Jean-Charles Grégoire, Gerard J. Holzmann, Doron Peled, What is SPIN SPIN is a general tool for the specification and formal verification of software for distributed systems It has been used to detect design errors in a wide range of applications such as abstract distributed algorithms data communications protocols operating systems code and telephone switching code The verifier can check for basic correctness properties such as absence of deadlock and race conditions logical completeness or unwarranted assumptions about the relative speeds of processes It can also check for more subtle system dependent correctness properties expressed in the syntax of Linear time Temporal Logic LTL The tool translates LTL formulae automatically into automata representations which can be used in an efficient on the fly verifications procedure This DIMACS volume presents the papers contributed to the second international workshop that was held on the SPIN verification system at Rutgers University in August 1996 The work covers theoretical and foundational studies of formal verifications empirical studies of the effectiveness of different types of algorithms significant practical applications of the SPIN verifier and discussions of extensions and revisions of the basic code This text will be of interest to those working in applications *Index to IEEE Publications* Institute of Electrical and Electronics Engineers, 1998 Issues for 1973 cover the entire IEEE technical literature **The SPIN Verification System** Jean-Charles Grégoire, 1997 What is Spin Spin is a general tool for the specification and formal verification of software for distributed systems It has been used to detect design errors in a wide range of applications such as abstract distributed algorithms data communications protocols operating systems code and telephone switching code The verifier can check for basic correctness properties such as absence of deadlock and race conditions logical completeness or unwarranted assumptions about the relative speeds of correctness properties expressed in the syntax of Linear time Temporal Logic LTL The tool tra *The SPIN Verification System*, 1997

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