

8. Design of Latches and flip flops: D-latch SR, D,JK, T

Aim: Design of Latches and flip flops (D-latch SR, D,JK, T) using Verilog and simulates the design

Apparatus required: - **Electronics Design Automation Tools used:** -

- Xilinx Spartan 3 FPGA
- Xilinx ISE Simulator tool
- Xilinx XST Synthesis tool
- Xilinx Project Navigator 8.1i
- JTAG cable
- Adaptor 5v/4A

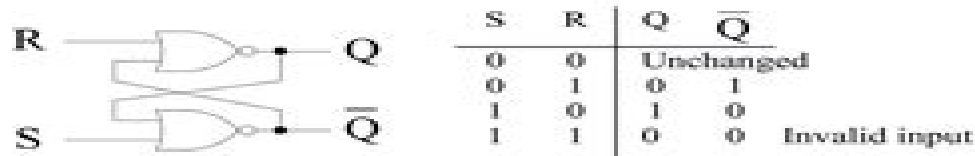
Theory:

LATCH AND FLIP-FLOP

Latch and flip-flop are memory devices and implemented using bistable circuit - its output will remain in either 0 or 1 state. The output state of a latch is controlled by its excitation input signals. A flip-flop (FF) is predominately controlled by a clock and its output state is determined by its excitation input signals. Note that if the clock is replaced by a gated control signal, the flip-flop becomes a gated latch.

a. RS (reset-set) latch circuit

When S (set) is set to 1, the output Q will be set to 1. Likewise, when R (reset) is set to 1, the output Q will be set to 0. It is invalid to set both S and R to 1.



NOR gate implementation



NAND gate implementation

Note that the input is active high for NOR gate implementation, whereas the input is active low for NAND gate implementation.

b. Clocked RS FF

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The Verilog PLI Handbook Stuart Sutherland, 2013-04-18 The Verilog Programming Language Interface commonly called the Verilog PU is one of the more powerful features of Verilog The PU provides a means for both hardware designers and software engineers to interface their own programs to commercial Verilog simulators Through this interface a Verilog simulator can be customized to perform virtually any engineering task desired Just a few of the common uses of the PU include interfacing Verilog simulations to C language models adding custom graphical tools to a simulator reading and writing proprietary file formats from within a simulation performing test coverage analysis during simulation and so forth The applications possible with the Verilog PLI are endless Intended audience this book is written for digital design engineers with a background in the Verilog Hardware Description Language and a fundamental knowledge of the C programming language It is expected that the reader has a basic knowledge of hardware engineering specifically digital design of ASIC and FPGA technologies Is familiar with the Verilog Hardware Description Language HDL and can write models of hardware circuits in Verilog can write simulation test fixtures in Verilog and can run at least one Verilog logic simulator Knows basic C language programming including the use of functions pointers structures and file I/O Explanations of the concepts and terminology of digital

Verification Methodology Manual for SystemVerilog Janick Bergeron, Eduard Cerny, Alan Hunter, Andy Nightingale, 2005-09-28 Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly Unique in its broad coverage of SystemVerilog advanced functional verification and the combination of the two

SystemVerilog For Design Stuart Sutherland, Simon Davidmann, Peter Flake, 2013-12-01 SystemVerilog is a rich set of extensions to the IEEE 1364 2001 Verilog Hardware Description Language Verilog HDL These extensions address two major aspects of HDL based design First modeling very large designs with concise accurate and intuitive code Second writing high level test programs to efficiently and effectively verify these large designs This book SystemVerilog for Design addresses the first aspect of the SystemVerilog extensions to Verilog Important modeling features are presented such as two state data types enumerated types user defined types structures unions and interfaces Emphasis is placed on the proper usage of these enhancements for simulation and synthesis A companion to this book SystemVerilog for Verification covers the second aspect of SystemVerilog

Verilog: Frequently Asked Questions Shivakumar S. Chonnad, Needamangalam B. Balachander, 2007-05-08 The Verilog Hardware Description Language was first introduced in 1984 Over the 20 year history of Verilog every Verilog engineer has developed his own personal bag of tricks for coding with Verilog These tricks enable modeling or verifying designs more easily and more accurately Developing this bag of tricks is often based on years of trial and error Through experience engineers learn that one specific coding style works best in some circumstances while in another situation a different coding style is best As with any high level language Verilog often provides engineers several

ways to accomplish a specific task Wouldn't it be wonderful if an engineer first learning Verilog could start with another engineer's bag of tricks without having to go through years of trial and error to decide which style is best for which circumstance That is where this book becomes an invaluable resource The book presents dozens of Verilog tricks of the trade on how to best use the Verilog HDL for modeling designs at various level of abstraction and for writing test benches to verify designs The book not only shows the correct ways of using Verilog for different situations it also presents alternate styles and discusses the pros and cons of these styles

Digital System Design and Verification Using System Verilog Mr. Rohit Manglik, 2024-03-06 EduGorilla Publication is a trusted name in the education sector committed to empowering learners with high quality study materials and resources Specializing in competitive exams and academic support EduGorilla provides comprehensive and well structured content tailored to meet the needs of students across various streams and levels

Digital VLSI Design with Verilog John Michael Williams, 2014-06-17 This book is structured as a step by step course of study along the lines of a VLSI integrated circuit design project The entire Verilog language is presented from the basics to everything necessary for synthesis of an entire 70 000 transistor full duplex serializer deserializer including synthesizable PLLs The author includes everything an engineer needs for in depth understanding of the Verilog language Syntax synthesis semantics simulation and test Complete solutions for the 27 labs are provided in the downloadable files that accompany the book For readers with access to appropriate electronic design tools all solutions can be developed simulated and synthesized as described in the book A partial list of design topics includes design partitioning hierarchy decomposition safe coding styles back annotation wrapper modules concurrency race conditions assertion based verification clock synchronization and design for test A concluding presentation of special topics includes System Verilog and Verilog AMS

System Verilog Assertions Handbook Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, 2005

Embedded Systems Handbook Richard Zurawski, 2018-09-03 Considered a standard industry resource the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications including those in automotive electronics industrial automated systems and building automation and control Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again Divided into two volumes to accommodate this growth the Embedded Systems Handbook Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews that explore cutting edge developments and deployments and identify potential trends This first self contained volume of the handbook Embedded Systems Design and Verification is divided into three sections It begins with a brief introduction to embedded systems design and verification It then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as

solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Those interested in taking their work with embedded systems to the network level should complete their study with the second volume *Network Embedded Systems* **Verilog** IEEE Standards Department,1995 *Reuse Methodology Manual for System-on-a-Chip Designs* Pierre Bricaud,2007-05-08 This revised and updated third edition outlines a set of best practices for creating reusable designs for use in an System on a Chip SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience of design teams in many companies around the world *Reuse Techniques for VLSI Design* Ralf Seepold,Arno Kunzmann,2012-12-06 Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design **VHDL Designer's Reference** Jean-Michel Bergé,Alain Fonkoua,Serge Maginot,Jacques Rouillard,2012-12-06 too vast too complex too grand for description John Wesley Powell 1870 discovering the Grand Canyon VHDL is a big world A beginner can be easily disappointed by the generality of this language This generality is explained by the large number of domains covered from specifications to logical simulation or synthesis To the very beginner VHDL appears as a kit He is quickly aware that his problem may be solved with VHDL but does not know how He does not even know how to start In this state of mind all the constraints that can be set to his modeling job by using a subset of the language or a given design methodology may be seen as a life preserver The success of the introduction of VHDL in a company depends on solutions to many questions that should be answered months before the first line of code is written Why choose VHDL Which VHDL tools should be chosen Which modeling methodology should be adopted How should the VHDL environment be customized What are the tricks Where are the traps What are the differences between VHDL and other competing HDLs Answers to these questions are organized according to different

concerns buying the tools organizing the environment and designing Decisions taken in each of these areas may have many consequences on the way to the acceptance and efficient use of VHDL in a company

Embedded Systems Handbook 2-Volume Set Richard Zurawski, 2018-10-08 During the past few years there has been an dramatic upsurge in research and development implementations of new technologies and deployments of actual solutions and technologies in the diverse application areas of embedded systems These areas include automotive electronics industrial automated systems and building automation and control Comprising 48 chapters and the contributions of 74 leading experts from industry and academia the Embedded Systems Handbook Second Edition presents a comprehensive view of embedded systems their design verification networking and applications The contributors directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews exploring new developments deployments and trends To accommodate the tremendous growth in the field the handbook is now divided into two volumes New in This Edition Processors for embedded systems Processor centric architecture description languages Networked embedded systems in the automotive and industrial automation fields Wireless embedded systems Embedded Systems Design and Verification Volume I of the handbook is divided into three sections It begins with a brief introduction to embedded systems design and verification The book then provides a comprehensive overview of embedded processors and various aspects of system on chip and FPGA as well as solutions to design challenges The final section explores power aware embedded computing design issues specific to secure embedded systems and web services for embedded devices Networked Embedded Systems Volume II focuses on selected application areas of networked embedded systems It covers automotive field industrial automation building automation and wireless sensor networks This volume highlights implementations in fast evolving areas which have not received proper coverage in other publications Reflecting the unique functional requirements of different application areas the contributors discuss inter node communication aspects in the context of specific applications of networked embedded systems

Verilog and SystemVerilog Gotchas Stuart Sutherland, Don Mills, 2010-04-30 In programming Gotcha is a well known term A gotcha is a language feature which if misused causes unexpected and in hardware design potentially disastrous behavior The purpose of this book is to enable engineers to write better Verilog SystemVerilog design and verification code and to deliver digital designs to market more quickly This book shows over 100 common coding mistakes that can be made with the Verilog and SystemVerilog languages Each example explains in detail the symptoms of the error the languages rules that cover the error and the correct coding style to avoid the error The book helps digital design and verification engineers to recognize these common coding mistakes and know how to avoid them Many of these errors are very subtle and can potentially cost hours or days of lost engineering time trying to find and debug the errors This book is unique because while there are many books that teach the language and a few that try to teach coding style no other book addresses how to recognize and avoid coding errors with these languages

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Microprocessor System Design using FPGAs Uwe Meyer-Baese, 2025-05-29 This textbook for courses in Embedded Systems introduces students to necessary concepts through a hands on approach It gives a great introduction to FPGA based microprocessor system design using state of the art boards tools and microprocessors from Altera Intel and Xilinx HDL based designs soft core parameterized cores Nios II and MicroBlaze and ARM Cortex A9 design are discussed compared and explored using many hand on designs projects Custom IP for HDMI coder Floating point operations and FFT bit swap are developed implemented tested and speed up is measured New additions in the second edition include bottom up and top down FPGA based Linux OS system designs for Altera Intel and Xilinx boards and application development running on the OS using modern popular programming languages Python Java and JavaScript HTML CSSs Downloadable files include all design examples such as basic processor synthesizable code for Xilinx and Altera tools for PicoBlaze MicroBlaze Nios II and ARMv7 architectures in VHDL and Verilog code as well as the custom IP projects For the three new OS enabled programming languages a substantial number of examples ranging from basic math and networking to image processing and video animations are provided Each Chapter has a substantial number of short quiz questions exercises and challenging projects

A Practical Guide to Analog Behavioral Modeling for IC System Design Paul A. Duran, 2012-11-14 A Practical Guide to Analog Behavioral Modeling for IC System Design presents a methodology for abstracting an IC system so that the designer can gain a macroscopic view of how sub systems interact as well as verify system functionality in various applications before committing to a design This will prevent problems that may be caused late in the design cycle by incompatibilities between the individual blocks that comprise the overall system This book will focus on the techniques of modelling IC systems through analog behavioral modeling and simulation It will investigate a practical approach by which designers can put together these systems to analyze topological and architectural issues to optimize IC system performance Highlights Discussions on modeling and simulation from SPICE to behavioral simulators Comparison of various hardware description languages and a discussion on the effects of language standardization Explanation on how to reduce time to market by decreasing design cycle time through modeling and simulation Contains more than 25 building block examples that can be used to construct mixed signal IC system models Analysis of 4 different IC systems using various levels of model detail This book is intended for the practicing engineer who would like to gain practical knowledge in applications of analog behavioral modelling for IC system design

SystemVerilog for Verification Chris Spear, Greg Tumbush, 2012-02-14 Based on the highly successful second edition this extended edition of SystemVerilog for Verification A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language providing hundreds of examples to clearly explain the concepts and basic fundamentals It contains materials for both the full time verification engineer and the student learning this valuable skill In the third edition authors Chris Spear and Greg Tumbush start with how to verify a design and then use that context to demonstrate the language features including the advantages and

disadvantages of different styles allowing readers to choose between alternatives This textbook contains end of chapter exercises designed to enhance students understanding of the material Other features of this revision include New sections on static variables print specifiers and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories the test registry and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification A Guide to Learning the Testbench Language Features Third Edition is suitable for use in a one semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers Fundamentals and Standards in Hardware Description Languages Jean Mermet,2012-12-06

The second half of this century will remain as the era of proliferation of electronic computers They did exist before but they were mechanical During next century they may perform other mutations to become optical or molecular or even biological Actually all these aspects are only fancy dresses put on mathematical machines This was always recognized to be true in the domain of software where machine or high level languages are more or less rigorous but immaterial variations of the universally accepted mathematical language aimed at specifying elementary operations functions algorithms and processes But even a mathematical machine needs a physical support and this is what hardware is all about The invention of hardware description languages HDL s in the early 60 s was an attempt to stay longer at an abstract level in the design process and to push the stage of physical implementation up to the moment when no more technology independant decisions can be taken It was also an answer to the continuous exponential growth of complexity of systems to be designed This problem is common to hardware and software and may explain why the syntax of hardware description languages has followed with a reasonable delay of ten years the evolution of the programming languages at the end of the 60 s they were Algol like a decade later Pascal like and now they are C or ADA like They have also integrated the new concepts of advanced software specification languages **Computer Hardware Description Languages and their Applications** D. Agnew,L. Claesen,R.

Camposano,2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification *FPGA Prototyping by*

SystemVerilog Examples Pong P. Chu, 2018-05-04 A hands on introduction to FPGA prototyping and SoC design This is the successor edition of the popular *FPGA Prototyping by Verilog Examples* text It follows the same learning by doing approach to teach the fundamentals and practices of HDL synthesis and FPGA prototyping The new edition uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP intellectual property cores integrate them into an SoC system on a chip framework realize the system on an FPGA prototyping board and verify the hardware and software operation The examples start with simple gate level circuits progress gradually through the RT register transfer level modules and lead to a functional embedded system with custom I O peripherals and hardware accelerators Although it is an introductory text the examples are developed in a rigorous manner and the derivations follow the strict design guidelines and coding practices used for large complex digital systems The book is completely updated and uses the SystemVerilog language which absorbs the Verilog language It presents the hardware design in the SoC context and introduces the hardware software co design concept Instead of treating examples as isolated entities the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software programmability and develop complex and interesting embedded system projects The new edition Adds four general purpose IP cores which are multi channel PWM pulse width modulation controller I2C controller SPI controller and XADC Xilinx analog to digital converter controller Introduces a music synthesizer constructed with a DDFS direct digital frequency synthesis module and an ADSR attack decay sustain release envelope generator Expands the original video controller into a complete stream based video subsystem that incorporates a video synchronization circuit a test pattern generator an OSD on screen display controller a sprite generator and a frame buffer Provides a detailed discussion on blocking and nonblocking statements and coding styles Describes basic concepts of software hardware co design with Xilinx MicroBlaze MCS soft core processor Provides an overview of bus interconnect and interface circuit Presents basic embedded system software development Suggests additional modules and peripherals for interesting and challenging projects *FPGA Prototyping by SystemVerilog Examples* makes a natural companion text for introductory and advanced digital design courses and embedded system courses It also serves as an ideal self teaching guide for practicing engineers who wish to learn more about this emerging area of interest

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