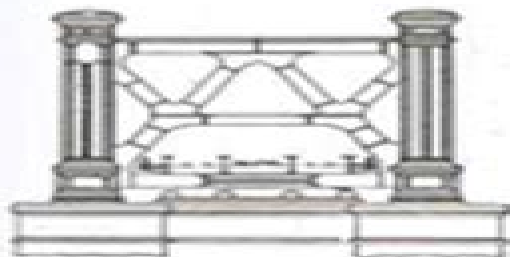
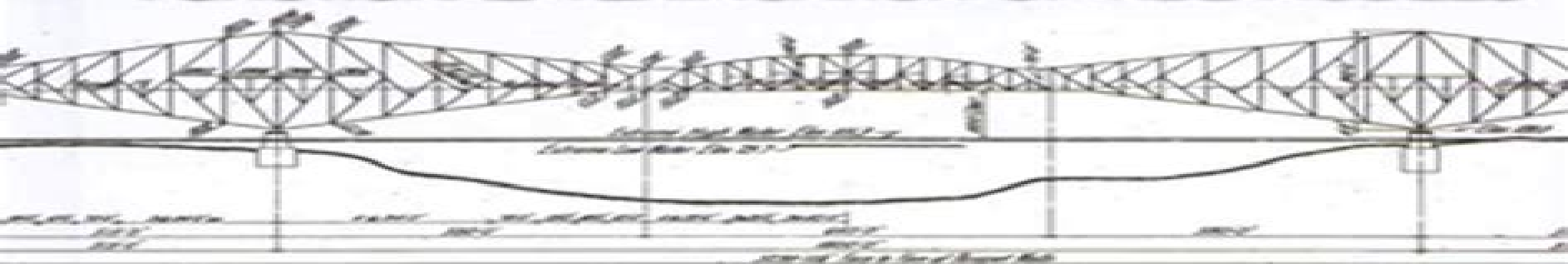


Writing Testbenches

FUNCTIONAL VERIFICATION OF HDL MODELS



by Janick Bergeron

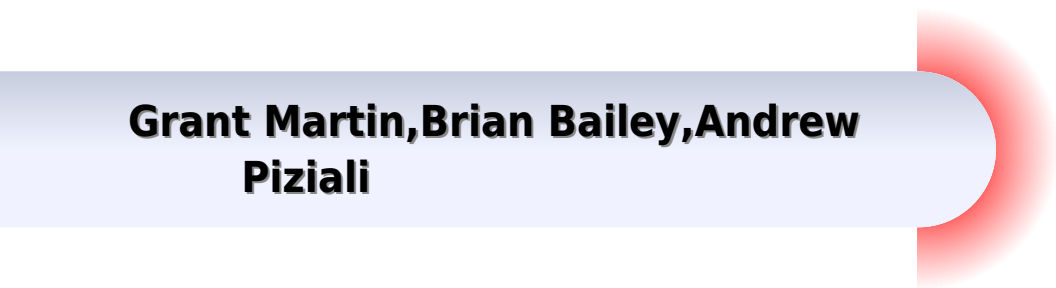


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Grant Martin, Brian Bailey, Andrew Piziali



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Writing Testbenches Janick Bergeron, 2007-05-08 CHAPTER 6 Architecting Testbenches 221 Reusable Verification Components 221 Procedural Interface 225 Development Process 226 Verilog Implementation 227 Packaging Bus Functional Models 228 Utility Packages 231 VHDL Implementation 237 Packaging Bus Functional Procedures 238 240 Creating a Test Harness 243 Abstracting the Client Server Protocol Managing Control Signals 246 Multiple Server Instances 247 Utility Packages 249 Autonomous Generation and Monitoring 250 Autonomous Stimulus 250 Random Stimulus 253 Injecting Errors 255 Autonomous Monitoring 255 258 Autonomous Error Detection Input and Output Paths 258 Programmable Testbenches 259 Configuration Files 260 Concurrent Simulations 261 Compile Time Configuration 262 Verifying Configurable Designs 263 Configurable Testbenches 265 Top Level Generics and Parameters 266 Summary 268 CHAPTER 7 Simulation Management 269 Behavioral Models 269 Behavioral versus Synthesizable Models 270 Example of Behavioral Modeling 271 Characteristics of a Behavioral Model 273 x Writing Testbenches Functional Verification of HDL Models Modeling Reset 276 Writing Good Behavioral Models 281 Behavioral Models Are Faster 285 The Cost of Behavioral Models 286 The Benefits of Behavioral Models 286 Demonstrating Equivalence 289 Pass or Fail 289 Managing Simulations 292 294 Configuration Management Verilog Configuration Management 295 VHDL Configuration Management 301 SDF Back Annotation 305 Output File Management 309 Regression 312 Running Regressions 313 Regression Management 314 Summary 316 APPENDIX A Coding Guidelines 317 Directory Structure 318 VHDL Specific 320 Verilog Specific 320 General Coding Guidelines 321 Comments 321 Layout 323 Syntax 326 Debugging 329 Naming Guidelines 329 Capitalization 330 Identifiers 332 Constants 334 334 HDL Specific Filenames 336 HDL Coding Guidelines 336 337 Structure 337 Layout **Writing Testbenches: Functional Verification of HDL Models** Janick Bergeron, 2003-02-28 The Second Edition of *Writing Testbenches Functional Verification of HDL Models* presents the latest verification techniques to produce fully functional first silicon ASICs systems on a chip SoC boards and entire systems From the Foreword Building on the first edition the most successful and popular contemporary verification textbook the author raises the verification level of abstraction by introducing coverage driven constrained random transaction level self checking testbenches all made possible through the introduction of hardware verification languages HVLs such as e from Verisity and OpenVera from Synopsys Harry Foster Chief Architect Verplex Systems Inc Topics included in the new Second Edition Discussions on OpenVera and e Approaches for writing constrainable random stimulus generators Strategies for making testbenches self checking A clear blueprint of a verification process that aims for first time success Recent advances in functional verification such as coverage driven verification process VHDL and Verilog language semantics The semantics are presented in new verification oriented languages Techniques for applying stimulus and monitoring the response of a design Behavioral modeling using non synthesizable constructs and coding style Updated for Verilog 2001 **Writing Testbenches: Functional Verification**

Of Hdl Models, 2E Bergeron, 2006-12-01 *Writing Testbenches: Functional Verification of HDL Models* Janick Bergeron, 2012-12-06

mental improvements during the same period What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough In the second edition of *Writing Testbenches* Bergeron raises the verification level of abstraction by introducing coverage driven constrained random transaction level self checking testbenches all made possible through the introduction of hardware verification languages HVLs such as e from Verisity and OpenVera from Synopsys The state of art methodologies described in *Writing Test benches* will contribute greatly to the much needed equivalent of a synthesis breakthrough in verification productivity I not only highly recommend this book but also I think it should be required reading by anyone involved in design and verification of today s ASIC SoCs and systems

Harry Foster Chief Architect Verplex Systems Inc xviii *Writing Testbenches Functional Verification of HDL Models* PREFACE

If you survey hardware design groups you will learn that between 60% and 80% of their effort is now dedicated to verification

The Functional Verification of Electronic Systems Brian Bailey, 2005-01-30 Addressing the need for full and accurate functional information during the design process this guide offers a comprehensive overview of functional verification from the points of view of leading experts at work in the electronic design industry

Real Chip Design and Verification Using Verilog and VHDL Ben Cohen, 2002 This book concentrates on common classes of hardware architectures and design problems and focuses on the process of transitioning design requirements into synthesizable HDL code Using his extensive wide ranging experience in computer architecture and hardware design as well as in his training and consulting work Ben provides numerous examples of real life designs illustrated with VHDL and Verilog code This code is shown in a way that makes it easy for the reader to gain a greater understanding of the languages and how they compare All code presented in the book is included on the companion CD along with other information such as application notes

Effective Functional Verification Srivatsa Vasudevan, 2006-07-29 *Effective Functional Verification* is organized into 4 parts The first part contains 3 chapters designed appeal to newcomers and experienced people to the field There is a survey of various verification methodologies and a discussion of them The second part with 3 chapters is targeted towards people in management and higher up on the experience ladders New verification engineers reading these chapters learn what is expected and how things work in verification Some case studies are also presented with analysis of proposed improvements The last two parts are the result of experience of several years It goes into how to optimize a verification plan and an environment and how to get results effectively Various subjects are discussed here to get the most out of a verification environment Lastly the appendix discusses some tool specifics to help remove repetitive work and also some tool specific guidelines While reading *Effective Functional Verification* one will be able to get a jump start on planning and executing a verification plan using the concepts presented

Hardware and Software: Verification and Testing Karen Yorav, 2008-02-02 This book constitutes the thoroughly refereed post workshop proceedings of the Third International Haifa Verification

Conference HVC 2007 held in Haifa Israel in October 2007 The 15 revised full papers presented together with 4 invited lectures were carefully reviewed and selected from 32 submissions The papers are organized in topical tracks on hardware verification model checking dynamic hardware verification merging formal and testing formal verification for software and software testing

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Embedded Systems Handbook Richard Zurawski, 2005-08-16 Embedded systems are nearly ubiquitous and books on individual topics or components of embedded systems are equally abundant Unfortunately for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink Until now The Embedded Systems Handbook is an oasis of information offering a mix of basic a

Open Verification Methodology Cookbook Mark Glasser, 2009-07-24 Functional verification is an art as much as a science It requires not only creativity and cunning but also a clear methodology to approach the problem The Open Verification Methodology OVM is a leading edge methodology for verifying designs at multiple levels of abstraction It brings together ideas from electrical systems and software engineering to provide a complete methodology for

verifying large scale System on Chip SoC designs OVM defines an approach for developing testbench architectures so they are modular configurable and reusable This book is designed to help both novice and experienced verification engineers master the OVM through extensive examples It describes basic verification principles and explains the essentials of transaction level modeling TLM It leads readers from a simple connection of a producer and a consumer through complete self checking testbenches It explains construction techniques for building configurable reusable testbench components and how to use TLM to communicate between them Elements such as agents and sequences are explained in detail

Introduction to VLSI Design Flow Sneha Saurabh, 2023-06-15 Chip designing is a complex task that requires an in depth understanding of VLSI design flow skills to employ sophisticated design tools and keeping pace with the bleeding edge semiconductor technologies This lucid textbook is focused on fulfilling these requirements for students as well as a refresher for professionals in the industry It helps the user develop a holistic view of the design flow through a well sequenced set of chapters on logic synthesis verification physical design and testing Illustrations and pictorial representations have been used liberally to simplify the explanation Additionally each chapter has a set of activities that can be performed using freely available tools and provide hands on experience with the design tools Review questions and problems are given at the end of each chapter to revise the concepts Recent trends and references are listed at the end of each chapter for further reading

System on Chip Design Languages Anne Mignotte, Eugenio Villar, Lynn Horobin, 2002-04-30 This volume is the third in a series It brings together a selection of the best papers from two international electronic design language conferences in 2001 The conferences are the Hardware Description Language Conference HDLCon in USA the Forum on Design Languages FDL in Europe The papers cover a range of topics including HDL specification and modelling languages including results from standardisation process from specialised languages such as VHDL and Verilog to general purpose languages such as C SystemC SpecC and Java Analogue and mixed signal specification and design System on chip real time and embedded specifications Real life experiences in using HDLs and EDA vendors point of view describing future design tools that utilise HDLs such as Web design environments simulation verification and synthesis tools The results presented in these papers will help researchers and practising engineers to keep abreast of developments in this rapidly evolving field

Assertion-Based Design Harry D. Foster, Adam C. Krolnik, David J. Lacey, 2012-12-06 There is much excitement in the design and verification community about assertion based design The question is who should study assertion based design The emphatic answer is both design and verification engineers What may be unintuitive to many design engineers is that adding assertions to RTL code will actually reduce design time while better documenting design intent Every design engineer should read this book Design engineers that add assertions to their design will not only reduce the time needed to complete a design they will also reduce the number of interruptions from verification engineers to answer questions about design intent and to address verification suite mistakes With design assertions in place the majority of the interruptions from verification

engineers will be related to actual design problems and the error feedback provided will be more useful to help identify design flaws A design engineer who does not add assertions to the RTL code will spend more time with verification engineers explaining the design functionality and intended interface requirements knowledge that is needed by the verification engineer to complete the job of testing the design

Component Design by Example Ben Cohen, 2001

Embedded and Ubiquitous Computing Edwin Sha, Sung-Kook Han, Cheng-Zhong Xu, Moon Hae Kim, Laurence T. Yang, Bin Xiao, 2006-10-06

This book constitutes the refereed proceedings of the International Conference on Embedded and Ubiquitous Computing EUC 2006 held in Seoul Korea August 2006 The book presents 113 revised full papers together with 3 keynote articles organized in topical sections on power aware computing security and fault tolerance agent and distributed computing wireless communications real time systems embedded systems multimedia and data management mobile computing network protocols middleware and P2P and more

Hardware Verification with System Verilog Mike Mintz, Robert Ekendahl, 2007-05-03

This is the second of our books designed to help the professional verifier manage complexity This time we have responded to a growing interest not only in object oriented programming but also in SystemVerilog The writing of this second handbook has been just another step in an ongoing masochistic endeavor to make your professional lives as painfree as possible The authors are not special people We have worked in several companies large and small made mistakes and generally muddled through our work There are many people in the industry who are smarter than we are and many coworkers who are more experienced However we have a strong desire to help We have been in the lab when we bring up the chips fresh from the fab with customers and sales breathing down our necks We've been through software 1 bring up and worked on drivers that had to work around bugs in production chips What we feel makes us unique is our combined broad experience from both the software and hardware worlds Mike has over 20 years of experience from the software world that he applies in this book to hardware verification Robert has over 12 years of experience with hardware verification with a focus on environments and methodology

Advanced Verification Techniques Leena Singh, Leonard Drucker, 2007-05-08

As chip size and complexity continues to grow exponentially the challenges of functional verification are becoming a critical issue in the electronics industry It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re spins and that the costs associated with functional verification are now outweighing the costs of chip design To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages Transaction based design and verification constrained random stimulus generation functional coverage analysis and assertion based verification are all techniques that advanced design and verification teams routinely use today Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract higher performance hardware and software models and to escape the limitations of RTL HDLs This new book *Advanced Verification Techniques* provides specific guidance for these advanced verification techniques The book includes

realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks

Stuart Swan Design Verification with E Samir Palnitkar, 2004 As part of the Modern Semiconductor Design series this book details a broad range of e based topics including modelling constraint driven test generation functional coverage and assertion checking *Writing Testbenches* Janick Bergeron, 2000-01-31

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