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Vtech Dect 60 Cs6219 Manual

Tobias Bleicker



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web the i 2c module contains an independent i 2c master logic and a i 2c slave logic which generates interrupts based on their events in the multi master systems the user software is simply partitioned into the master controller and the slave controller when the i 2c master logic is active the slave logic also remains active detecting the

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web i2c master h this header contains i o definitions selection and timing clock speed settings used for the master i2c interface this file also includes prototypes of master i2c functions i2c master c this source file contains master i2c function implementations file

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web i2c module modes and features the i2c module provides the following operational modes and features master mode slave mode with byte nacking multi master mode dedicated receive and transmit buffers up to four dedicated slave address registers 1

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web the i 2 c master is byte oriented and interrupt based the number of interrupts generated is kept at a minimum by automatic handling of most incidents the software driver complexity and code size are reduced by auto triggering of operations and a special smart mode which can be enabled by the smart mode enable bit in the control b register

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the final fantasy xi wings of the goddess

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