

Qiaoyan Yu · Paul Ampadu

Transient and Permanent Error Control for Networks-on-Chip

Transient And Permanent Error Control For Networks On Chip

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Transient And Permanent Error Control For Networks On Chip:

Transient and Permanent Error Control for Networks-on-Chip Qiaoyan Yu, Paul Ampadu, 2011-11-18 This book addresses reliability and energy efficiency of on chip networks using cooperative error control It describes an efficient way to construct an adaptive error control codec capable of tracking noise conditions and adjusting the error correction strength at runtime Methods are also presented to tackle joint transient and permanent error correction exploiting the redundant resources already available on chip A parallel and flexible network simulator is also introduced which facilitates examining the impact of various error control methods on network on chip performance

Transient and Permanent Error Control for Networks-On-Chip Springer, 2012-05-01 Error Control for Network-on-Chip Links Bo Fu, Paul Ampadu, 2011-10-09 This book provides readers with a comprehensive review of the state of the art in error control for Network on Chip NOC links Coverage includes detailed description of key issues in NOC error control faced by circuit and system designers as well as practical error control techniques to minimize the impact of these errors on system performance

Asynchronous On-Chip Networks and Fault-Tolerant Techniques Wei Song, Guangda Zhang, 2022-05-10 Asynchronous On Chip Networks and Fault Tolerant Techniques is the first comprehensive study of fault tolerance and fault caused deadlock effects in asynchronous on chip networks aiming to overcome these drawbacks and ensure greater reliability of applications As a promising alternative to the widely used synchronous on chip networks for multicore processors asynchronous on chip networks can be vulnerable to faults even if they can deliver the same performance with much lower energy and area compared with their synchronous counterparts faults can not only corrupt data transmission but also cause a unique type of deadlock By adopting a new redundant code along with a dynamic fault detection and recovery scheme the authors demonstrate that asynchronous on chip networks can be efficiently hardened to tolerate both transient and permanent faults and overcome fault caused deadlocks This book will serve as an essential guide for researchers and students studying interconnection networks fault tolerant computing asynchronous system design circuit design and on chip networking as well as for professionals interested in designing fault tolerant and high throughput asynchronous circuits

Reliability, Availability and Serviceability of Networks-on-Chip Érika Cota, Alexandre de Moraes Amory, Marcelo Soares

Lubaszewski, 2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the art on chip communication architectures

Transient and Permanent Error Management for Networks-on-chip Qiaoyan Yu, 2011 Reliability has become one of the most important metrics for on chip communications infrastructures in nanoscale technologies Reduced supply voltages and high clock frequency exacerbate the impact of noise sources such as particle strikes and crosstalk which can cause transient errors in transmitted data Manufacturing defects and aging issues

can cause permanent errors in the communication links. The modularity of the Networks on Chip NoCs approach facilitates the exploration of error control techniques for on chip interconnects and many cores systems. Unfortunately error control is not free. Worst case error management methods are simple but waste energy and bandwidth in favorable noise conditions. Consequently cost effective techniques for improving link error resilience are needed. In this work we propose configurable error control methods to tackle variable transient errors and exploit existing transient error control redundancy for permanent error management achieving high reliability and low average energy consumption with minor area overhead. To adapt to the variable transient error rates a configurable error control coding ECC scheme is proposed for datalink layer transient error management. The proposed method can adjust both error detection and error correction capability at runtime by varying the number of redundant wires for parity check bits. The obtained error resilience makes the proposed method suitable for a range of link error rates. Configuring the number of redundant wires to match the noise conditions reduces the average energy consumption in the ECC codec and interconnect link. A hardware efficient implementation for the configurable ECC is presented as well. We integrate the error control techniques in the datalink and physical layers to co manage transient and permanent errors. Infrequently used redundant wires for the configurable ECC are utilized as spare wires to replace permanently unusable links. To maintain the transient and permanent error co management capability as noise conditions change we propose a packet re organization algorithm combined with shortening error control coding method. This method reduces the need for energy consuming fault tolerant routing minimizing latency and energy overhead induced by error control. This co management method is suitable for NoCs operating in variable noise conditions with a small number of permanently unusable wires. To further improve energy efficiency the adaptation on ECC is extended to the network layer. We employ end to end error control in the network layer in low noise conditions and enhance the error control capability in high noise conditions by adding hop to hop error control in the datalink layer. A protocol that boosts or reduces error control strength is presented to support runtime seamless ECC mode switching. Simply combining end to end error control with hop to hop error control significantly increases energy consumption. To address this issue we apply the concept of product codes to the dual layer error control. The hop to hop error control is designed to be compatible with one dimension of the product code. Consequently the dual layer cooperative error control can switch error control modes without interrupting normal NoC operation achieving high reliability and energy efficiency in a wide range of link error rates. To evaluate performance and energy consumption of different error control methods on a large size NoC we propose a flexible parallel NoC simulator. Plug and play error control coding ECC insertion and some typical error control codecs have been implemented in the simulator. The flexible fault injection environment provided by our simulator assists error control exploration for specific purposes. In addition we use C and message passing interface MPI languages to schedule parallel simulation on a multiprocessor server addressing the prohibitive simulation time and system resource challenges caused by

the large number of communicating nodes and extensive number of simulation variables Leaves iv vi Network-on-Chip
Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration
Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

Reconfigurable Networks-on-Chip Sao-Jie Chen, Ying-Cherng Lan, Wen-Chung Tsai, Yu-Hen Hu, 2011-12-16 This book provides a comprehensive survey of recent progress in the design and implementation of Networks on Chip It addresses a wide spectrum of on chip communication problems ranging from physical network to application layers Specific topics that are explored in detail include packet routing resource arbitration error control correction application mapping and communication scheduling Additionally a novel bi directional communication channel NoC BiNoC architecture is described with detailed explanation Written for practicing engineers in need of practical knowledge about the design and implementation of networks on chip Includes tutorial like details to introduce readers to a diverse range of NoC designs as well as in depth analysis for designers with NoC experience to explore advanced issues Describes a variety of on chip

communication architectures including a novel bi directional communication channel NoC From the Foreword Overall this book shows important advances over the state of the art that will affect future system design as well as R D in tools and methods for NoC design It represents an important reference point for both designers and electronic design automation researchers and developers Giovanni De Micheli *Designing 2D and 3D Network-on-Chip Architectures* Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies **'Advances in Microelectronics: Reviews', Vol_1** Sergey Yurish,2017-12-24 The 1st volume of Advances in Microelectronics Reviews Book Series contains 19 chapters written by 72 authors from academia and industry from 16 countries With unique combination of information in each volume the Advances in Microelectronics Reviews Book Series will be of value for scientists and engineers in industry and at universities In order to offer a fast and easy reading of the state of the art of each topic every chapter in this book is independent and self contained All chapters have the same structure first an introduction to specific topic under study second particular field description including sensing applications Each of chapter is ending by well selected list of references with books journals conference proceedings and web sites This book ensures that readers will stay at the cutting edge of the field and get the right and effective start point and road map for the further researches and developments **Issues in Electronic Circuits, Devices, and Materials: 2012 Edition** ,2013-01-10 Issues in Electronic Circuits Devices and Materials 2012 Edition is a ScholarlyEditions eBook that delivers timely authoritative and comprehensive information about Lasers and Photonics The editors have built Issues in Electronic Circuits Devices and Materials 2012 Edition on the vast information databases of ScholarlyNews You can expect the information about Lasers and Photonics in this eBook to be deeper than what you can access anywhere else as well as consistently reliable authoritative informed and relevant The content of Issues in Electronic Circuits Devices and Materials 2012 Edition has been produced by the world s leading scientists engineers analysts research institutions and companies All of the content is from peer reviewed sources and all of it is written assembled and edited by the editors at ScholarlyEditions and available exclusively from us You now have a source you can cite with authority confidence and credibility More information is available at <http://www.ScholarlyEditions.com> *Design Technologies for Green and Sustainable Computing Systems* Partha Pratim Pande,Amlan Ganguly,Krishnendu Chakrabarty,2013-07-17 This book provides a comprehensive guide to the design of sustainable and green computing systems GSC Coverage includes important breakthroughs in various aspects of GSC including multi core architectures interconnection technology data centers high performance computing HPC and sensor networks The authors address the challenges of power efficiency and sustainability

in various contexts including system design computer architecture programming languages compilers and networking

Designing Reliable and Efficient Networks on Chips Srinivasan Murali, 2009-05-26 Developing NoC based interconnect tailored to a particular application domain satisfying the application performance constraints with minimum power area overhead is a major challenge With technology scaling as the geometries of on chip devices reach the physical limits of operation another important design challenge for NoCs will be to provide dynamic run time support against permanent and intermittent faults that can occur in the system The purpose of Designing Reliable and Efficient Networks on Chips is to provide state of the art methods to solve some of the most important and time intensive problems encountered during NoC design

Networks on Chips Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today s semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems These highly complex systems on chips demand new approaches to connect and manage the communication between on chip processing and storage components and networks on chips NoCs provide a powerful solution This book is the first to provide a unified overview of NoC technology It includes in depth analysis of all the on chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and solutions Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends An integrated presentation not currently available in any other book A thorough introduction to current design methodologies and chips designed with NoCs

Managing Temperature Effects in Nanoscale Adaptive Systems David Wolpert, Paul Ampadu, 2011-08-31 This book discusses new techniques for detecting controlling and exploiting the impacts of temperature variations on nanoscale circuits and systems A new sensor system is described that can determine the temperature dependence as well as the operating temperature to improve system reliability A new method is presented to control a circuit s temperature dependence by individually tuning pull up and pull down networks to their temperature insensitive operating points This method extends the range of supply voltages that can be made temperature insensitive achieving insensitivity at nominal voltage for the first time

Dependable Computing Carlos Alberto Maziero, 2005-10-11 This book constitutes the refereed proceedings of the Second Latin American Symposium on Dependable Computing LADC 2005 held in Salvador Brazil in October 2005 The 16 revised full papers presented together with 3 invited talks and outlines of 2 workshops and 3 tutorials were carefully reviewed and selected from 39 submissions The papers are organized in topical sections on evaluation certification modelling embedded systems time and distributed systems algorithms

Interconnect-Centric Design for Advanced SOC and NOC Jari Nurmi, H. Tenhunen, J. Isoaho, Axel Jantsch, 2006-03-20 In Interconnect centric Design for Advanced SoC and NoC we have tried to create a comprehensive understanding about on chip interconnect characteristics design methodologies layered views on different abstraction levels and finally about applying the interconnect centric design in system on chip design Traditionally on chip communication

design has been done using rather ad hoc and informal approaches that fail to meet some of the challenges posed by next generation SOC designs such as performance and throughput power and energy reliability predictability synchronization and management of concurrency To address these challenges it is critical to take a global view of the communication problem and decompose it along lines that make it more tractable We believe that a layered approach similar to that defined by the communication networks community should also be used for on chip communication design The design issues are handled on physical and circuit layer logic and architecture layer and from system design methodology and tools point of view Formal communication modeling and refinement is used to bridge the communication layers and network centric modeling of multiprocessor on chip networks and socket based design will serve the development of platforms for SoC and NoC integration Interconnect centric Design for Advanced SoC and NoC is concluded by two application examples interconnect and memory organization in SoCs for advanced set top boxes and TV and a case study in NoC platform design for more generic applications

Network-on-Chip Architectures Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R. Das, 2009-09-18

2 The Cell Processor from Sony Toshiba and IBM STI 3 and the Sun UltraSPARC T1 formerly codenamed Niagara 4 signal the growing popularity of such systems Furthermore Intel's very recently announced 80 core TeraFLOP chip 5 exemplifies the irreversible march toward many core systems with tens or even hundreds of processing elements

1 2 The Dawn of the Communication Centric Revolution The multi core thrust has ushered the gradual displacement of the computation centric design model by a more communication centric approach

6 The large sophisticated monolithic modules are giving way to several smaller simpler processing elements working in tandem This trend has led to a surge in the popularity of multi core systems which typically manifest themselves in two distinct incarnations heterogeneous Multi Processor Systems on Chip MPSoC and homogeneous Chip Multi Processors CMP The SoC philosophy revolves around the technique of Platform Based Design PBD 7 which advocates the reuse of Intellectual Property IP cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations The appeal of such a modular approach lies in the substantially reduced Time To Market TTM incubation period which is a direct outcome of lower circuit complexity and reduced design effort The whole system can now be viewed as a diverse collection of pre-existing IP components integrated on a single die

Principles and Practices of Interconnection Networks William James Dally, Brian Patrick Towles, 2004-03-06

One of the greatest challenges faced by designers of digital systems is optimizing the communication and interconnection between system components Interconnection networks offer an attractive and economical solution to this communication crisis and are fast becoming pervasive in digital systems Current trends suggest that this communication bottleneck will be even more problematic when designing future generations of machines Consequently the anatomy of an interconnection network router and science of interconnection network design will only grow in importance in the coming years This book offers a detailed and comprehensive presentation of the basic principles of interconnection network design

clearly illustrating them with numerous examples chapter exercises and case studies It incorporates hardware level descriptions of concepts allowing a designer to see all the steps of the process from abstract design to concrete implementation Case studies throughout the book draw on extensive author experience in designing interconnection networks over a period of more than twenty years providing real world examples of what works and what doesn't Tightly couples concepts with implementation costs to facilitate a deeper understanding of the tradeoffs in the design of a practical network A set of examples and exercises in every chapter help the reader to fully understand all the implications of every design decision

MULTICORE SYSTEMS ON-CHIP Ben Abadallah Abderazek, 2010-08-01 Conventional on chip communication design mostly use ad hoc approaches that fail to meet the challenges posed by the next generation MultiCore Systems on chip MCSoc designs These major challenges include wiring delay predictability diverse interconnection architectures and power dissipation A Network on Chip NoC paradigm is emerging as the solution for the problems of interconnecting dozens of cores into a single system on chip However there are many problems associated with the design of such systems These problems arise from non scalable global wire delays failure to achieve global synchronization and difficulties associated with non scalable bus based functional interconnects The book consists of three parts with each part being subdivided into four chapters The first part deals with design and methodology issues The architectures used in conventional methods of MCSocs design and custom multiprocessor architectures are not flexible enough to meet the requirements of different application domains and not scalable enough to meet different computation needs and different complexities of various applications Several chapters of the first part will emphasize on the design techniques and methodologies The second part covers the most critical part of MCSocs design the interconnections One approach to addressing the design methodologies is to adopt the so called reusability feature to boost design productivity In the past years the primitive design units evolved from transistors to gates finite state machines and processor cores The network on chip paradigm offers this attractive property for the future and will be able to close the productivity gap The last part of this book delves into MCSocs validations and optimizations A more qualitative approach of system validation is based on the use of formal techniques for hardware design The main advantage of formal methods is the possibility to prove the validity of essential design requirements As formal languages have a mathematical foundation it is possible to formally extract and verify these desired properties of the complete abstract state space Online testing techniques for identifying faults that can lead to system failure are also surveyed Emphasis is given to analytical redundancy based techniques that have been developed for fault detection and isolation in the automatic control area

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