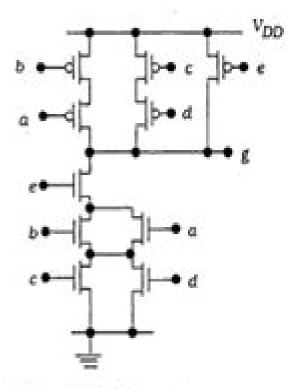
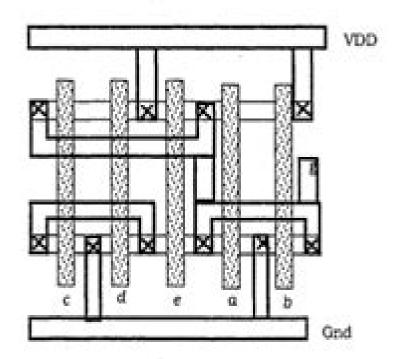
[3.16] The OAI function is

$$g = (a+b) \cdot (c+d) \cdot e$$

This is obtained from the CMOS circuit shown below. The placement of the inputs has be chosen to facilitate the layout.





Problem [3.16] Circuit

Mladen Božanić, Saurabh Sinha

Transistor-Level Layout of Integrated Circuits Jan Schneider, 2014-09-10 Description and analysis of algorithms for the transistor level layout of CMOS cells Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation Bertrand Hochet, Antonio J. Acosta, 2002-08-28 This book constitutes the refereed proceedings of the 12th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2002 held in Seville Spain in September 2002 The 37 revised full papers and 12 poster papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on arithmetics low level modeling and characterization asynchronous and adiabatic techniques CAD tools and algorithms timing gate level modeling and design and communications modeling and activity reduction Physical Design for 3D Integrated Circuits Aida Todri-Sanial, Chuan Seng Tan, 2017-12-19 Physical Design for 3D Integrated Circuits reveals how to effectively and optimally design 3D integrated circuits ICs It also analyzes the design tools for 3D circuits while exploiting the benefits of 3D technology The book begins by offering an overview of physical design challenges with respect to conventional 2D circuits and then each chapter delivers an in depth look at a specific physical design topic This comprehensive reference Contains extensive coverage of the physical design of 2 5D 3D ICs and monolithic 3D ICs Supplies state of the art solutions for challenges unique to 3D circuit design Features contributions from renowned experts in their respective fields Physical Design for 3D Integrated Circuits provides a single convenient source of cutting edge information for those pursuing 2 5D 3D technology **Integrated Circuit and** System Design Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou, 2004-09-07 This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation PATMOS 2004 held in Santorini Greece in September 2004 The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted. The papers are organized in topical sections on buses and communication circuits and devices low power issues architectures asynchronous circuits systems design interconnect and physical design security and safety low power processing digital design and modeling and simulation **Digital Integrated** Circuit Design Hubert Kaeslin, 2008-04-28 This practical tool independent guide to designing digital circuits takes a unique top down approach reflecting the nature of the design process in industry Starting with architecture design the book comprehensively explains the why and how of digital circuit design using the physics designers need to know and no more

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