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Editors

Three Dimensional System Integration

IC Stacking Process and Design

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Three Dimensional System Integration Ic Stacking Process And Design

Peter Ramm,James Jian-Qiang Lu,Maaike M. V. Taklo

Three Dimensional System Integration Ic Stacking Process And Design:

Three Dimensional System Integration Antonis Papanikolaou,Dimitrios Soudris,Riko Radojcic,2010-12-07 Three dimensional 3D integrated circuit IC stacking is the next big step in electronic system integration It enables packing more functionality as well as integration of heterogeneous materials devices and signals in the same space volume This results in consumer electronics e g mobile handheld devices which can run more powerful applications such as full length movies and 3D games with longer battery life This technology is so promising that it is expected to be a mainstream technology a few years from now less than 10 15 years from its original conception To achieve this type of end product changes in the entire manufacturing and design process of electronic systems are taking place This book provides readers with an accessible tutorial on a broad range of topics essential to the non expert in 3D System Integration It is an invaluable resource for anybody in need of an overview of the 3D manufacturing and design chain *Three-Dimensional Integrated Circuit Design* Vasilis F. Pavlidis,Ioannis Savidis,Eby G. Friedman,2017-07-04 Three Dimensional Integrated Circuit Design Second Eition expands the original with more than twice as much new content adding the latest developments in circuit models temperature considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization **3D IC Stacking Technology** Banqiu Wu,Ajay Kumar,Sesh Ramaswami,2011-07-07 The latest advances in three dimensional integrated circuit stacking technology With a focus on industrial applications 3D IC Stacking Technology offers comprehensive coverage of design test and fabrication processing methods for three dimensional device integration Each chapter in this authoritative guide is written by industry experts and details a separate fabrication step Future industry applications and cutting edge design potential are also discussed This is an essential resource for semiconductor engineers and portable device designers 3D IC Stacking Technology covers High density through silicon stacking TSS technology Practical design ecosystem for heterogeneous 3D IC products Design automation and TCAD tool solutions for through silicon via TSV based 3D IC stack

Process integration for TSV manufacturing High aspect ratio silicon etch for TSV Dielectric deposition for TSV Barrier and seed deposition Copper electrodeposition for TSV Chemical mechanical polishing for TSV applications Temporary and permanent bonding Assembly and test aspects of TSV technology **Design of 3D Integrated Circuits and Systems** Rohit Sharma,2018-09-03 Three dimensional 3D integration of microsystems and subsystems has become essential to the future of semiconductor technology development 3D integration requires a greater understanding of several interconnected systems stacked over each other While this vertical growth profoundly increases the system functionality it also exponentially increases the design complexity Design of 3D Integrated Circuits and Systems tackles all aspects of 3D integration including 3D circuit and system design new processes and simulation techniques alternative communication schemes for 3D circuits and systems application of novel materials for 3D systems and the thermal challenges to restrict power dissipation and improve performance of 3D systems Containing contributions from experts in industry as well as academia this authoritative text Illustrates different 3D integration approaches such as die to die die to wafer and wafer to wafer Discusses the use of interposer technology and the role of Through Silicon Vias TSVs Presents the latest improvements in three major fields of thermal management for multiprocessor systems on chip MPSoCs Explores ThruChip Interface TCI NAND flash memory stacking and emerging applications Describes large scale integration testing and state of the art low power testing solutions Complete with experimental results of chip level 3D integration schemes tested at IBM and case studies on advanced complementary metal oxide semiconductor CMOS integration for 3D integrated circuits ICs Design of 3D Integrated Circuits and Systems is a practical reference that not only covers a wealth of design issues encountered in 3D integration but also demonstrates their impact on the efficiency of 3D systems **Handbook of 3D Integration, Volume 3** Philip Garrou,Mitsumasa Koyanagi,Peter Ramm,2014-04-22 Edited by key figures in 3D integration and written by top authors from high tech companies and renowned research institutions this book covers the intricate details of 3D process technology As such the main focus is on silicon via formation bonding and debonding thinning via reveal and backside processing both from a technological and a materials science perspective The last part of the book is concerned with assessing and enhancing the reliability of the 3D integrated devices which is a prerequisite for the large scale implementation of this emerging technology Invaluable reading for materials scientists semiconductor physicists and those working in the semiconductor industry as well as IT and electrical engineers Handbook of 3D Integration, Volume 4 Paul D. Franzon,Erik Jan Marinissen,Muhannad S. Bakir,2019-01-25 This fourth volume of the landmark handbook focuses on the design testing and thermal management of 3D integrated circuits both from a technological and materials science perspective Edited and authored by key contributors from top research institutions and high tech companies the first part of the book provides an overview of the latest developments in 3D chip design including challenges and opportunities The second part focuses on the test methods used to assess the quality and reliability of the 3D integrated circuits while the third and final part deals with thermal management and

advanced cooling technologies and their integration **Three-Dimensional Integrated Circuit Design** Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2009-12-02 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs **Three-Dimensional Integration of Semiconductors** Kazuo Kondo,Morihiro Kada,Kenji Takahashi,2015-12-09 This book starts with background concerning three dimensional integration including their low energy consumption and high speed image processing and then proceeds to how to construct them and which materials to use in particular situations The book covers numerous applications including next generation smart phones driving assistance systems capsule endoscopes homing missiles and many others The book concludes with recent progress and developments in three dimensional packaging as well as future prospects *Advanced Interconnects for ULSI Technology* Mikhail Baklanov,Paul S. Ho,Ehrenfried Zschech,2012-04-02 Finding new materials for copper low k interconnects is critical to the continuing development of computer chips While copper low k interconnects have served well allowing for the creation of Ultra Large Scale Integration ULSI devices which combine over a billion transistors onto a single chip the increased resistance and RC delay at the smaller scale has become a significant factor affecting chip performance Advanced Interconnects for ULSI Technology is dedicated to the materials and methods which might be suitable replacements It covers a broad range of topics from physical principles to design fabrication characterization and application of new materials for nano interconnects and discusses Interconnect functions characterisations electrical properties and wiring requirements Low k materials fundamentals advances and mechanical properties Conductive layers and barriers Integration and reliability including mechanical reliability electromigration and electrical breakdown New approaches including 3D optical wireless interchip and carbon based interconnects Intended for postgraduate students and researchers in academia and industry this book provides a critical overview of the enabling

technology at the heart of the future development of computer chips **3D Microelectronic Packaging** Yan Li,Deepak Goyal,2020-11-23 This book offers a comprehensive reference guide for graduate students and professionals in both academia and industry covering the fundamentals architecture processing details and applications of 3D microelectronic packaging It provides readers an in depth understanding of the latest research and development findings regarding this key industry trend including TSV die processing micro bumps for LMI and MMI direct bonding and advanced materials as well as quality reliability fault isolation and failure analysis for 3D microelectronic packages Images tables and didactic schematics are used to illustrate and elaborate on the concepts discussed Readers will gain a general grasp of 3D packaging quality and reliability concerns and common causes of failure and will be introduced to developing areas and remaining gaps in 3D packaging that can help inspire future research and development **Three-Dimensional Design Methodologies for Tree-based FPGA Architecture** Vinod Pangracious,Zied Marrakchi,Habib Mehrez,2015-06-25 This book focuses on the development of 3D design and implementation methodologies for Tree based FPGA architecture It also stresses the needs for new and augmented 3D CAD tools to support designs such as the design for 3D to manufacture high performance 3D integrated circuits and reconfigurable FPGA based systems This book was written as a text that covers the foundations of 3D integrated system design and FPGA architecture design It was written for the use in an elective or core course at the graduate level in field of Electrical Engineering Computer Engineering and Doctoral Research programs No previous background on 3D integration is required nevertheless fundamental understanding of 2D CMOS VLSI design is required It is assumed that reader has taken the core curriculum in Electrical Engineering or Computer Engineering with courses like CMOS VLSI design Digital System Design and Microelectronics Circuits being the most important It is accessible for self study by both senior students and professionals alike **Advances In 3d Integrated Circuits And Systems** Hao Yu,Chuan Seng Tan,2015-08-28 3D integration is an emerging technology for the design of many core microprocessors and memory integration This book Advances in 3D Integrated Circuits and Systems is written to help readers understand 3D integrated circuits in three stages device basics system level management and real designs Contents presented in this book include fabrication techniques for 3D TSV and 2 5D TSI device modeling physical designs thermal power and I O management and 3D designs of sensors I Os multi core processors and memory Advanced undergraduates graduate students researchers and engineers may find this text useful for understanding the many challenges faced in the development and building of 3D integrated circuits and systems *Through Silicon Vias* Brajesh Kumar Kaushik,Vobulapuram Ramesh Kumar,Manoj Kumar Majumder,Arsalan Alam,2016-11-30 Recent advances in semiconductor technology offer vertical interconnect access via that extend through silicon popularly known as through silicon via TSV This book provides a comprehensive review of the theory behind TSVs while covering most recent advancements in materials models and designs Furthermore depending on the geometry and physical configurations different electrical equivalent models for Cu carbon nanotube CNT and graphene

nanoribbon GNR based TSVs are presented Based on the electrical equivalent models the performance comparison among the Cu CNT and GNR based TSVs are also discussed **Physical Design for 3D Integrated Circuits** Aida Todri-Sanial,Chuan Seng Tan,2017-12-19 Physical Design for 3D Integrated Circuits reveals how to effectively and optimally design 3D integrated circuits ICs It also analyzes the design tools for 3D circuits while exploiting the benefits of 3D technology The book begins by offering an overview of physical design challenges with respect to conventional 2D circuits and then each chapter delivers an in depth look at a specific physical design topic This comprehensive reference Contains extensive coverage of the physical design of 2 5D 3D ICs and monolithic 3D ICs Supplies state of the art solutions for challenges unique to 3D circuit design Features contributions from renowned experts in their respective fields Physical Design for 3D Integrated Circuits provides a single convenient source of cutting edge information for those pursuing 2 5D 3D technology Wafer Level 3-D ICs Process Technology Chuan Seng Tan,Ronald J. Gutmann,L. Rafael Reif,2009-06-29 Three dimensional 3D integration is clearly the simplest answer to most of the semiconductor industry s vexing problems heterogeneous integration and red tions of power form factor delay and even cost Conceptually the power latency and form factor of a system with a xed number of transistors all scale roughly linearly with the diameter of the smallest sphere enclosing frequently interacting devices This clearly provides the fundamental motivation behind 3D technologies which vertically stack several strata of device and interconnect layers with high vertical interconnectivity In addition the ability to vertically stack strata with vergent and even incompatible process ows provides for low cost and low parasitic integration of diverse technologies such as sensors energy scavengers nonvolatile memory dense memory fast memory processors and RF layers These capabilities coupled with today s trends of increasing levels of integrated functionality lower power smaller form factor increasingly divergent process ows and functional diversi cation would seem to make 3D technologies a natural choice for most of the semiconductor industry Since the concept of vertical integration of different strata has been around for over 20 years why aren t vertically stacked strata endemic to the semiconductor industry The simple answer to this question is that in the past the 3D advantages while interesting were not necessary due to the tremendous opportunities offered by geometric scaling In addition even when the global interconnect problem of high performance single core processors seemed insurmountable without inno tions such as 3D alternative architectural solutions such as multicores could eff tivelydelaybutnoteliminatetheneedfor3D 3D Integration in VLSI Circuits Katsuyuki Sakuma,2018-04-17 Currently the term 3D integration includes a wide variety of different integration methods such as 2 5 dimensional 2 5D interposer based integration 3D integrated circuits 3D ICs 3D systems in package SiP 3D heterogeneous integration and monolithic 3D ICs The goal of this book is to provide readers with an understanding of the latest challenges and issues in 3D integration TSVs are not the only technology element needed for 3D integration There are numerous other key enabling technologies required for 3D integration and the speed of the development in this emerging field is very rapid To provide readers with state of the

art information on 3D integration research and technology developments each chapter has been contributed by some of the world s leading scientists and experts from academia research institutes and industry from around the globe Covers chip wafer level 3D integration technology memory stacking reconfigurable 3D and monolithic 3D IC Discusses the use of silicon interposer and organic interposer Presents architecture design and technology implementations for 3D FPGA integration Describes oxide bonding Cu SiO2 hybrid bonding adhesive bonding and solder bonding Addresses the issue of thermal dissipation in 3D integration *Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology* Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **Applied Reconfigurable Computing** Kentaro Sano,Dimitrios Soudris,Michael Hübner,Pedro C. Diniz,2015-03-30 This book constitutes the refereed proceedings of the 11th International Symposium on Applied Reconfigurable Computing ARC 2015 held in Bochum Germany in April 2015 The 23 full papers and 20 short papers presented in this volume were carefully reviewed and selected from 85 submissions They are organized in topical headings named architecture and modeling tools and compilers systems and applications network on a chip cryptography applications extended abstracts of posters In addition the book contains invited papers on funded R D running and completed projects and Horizon 2020 funded projects

Reconfigurable Logic Pierre-Emmanuel Gaillardon,2018-09-03 During the last three decades reconfigurable logic has been growing steadily and can now be found in many different fields Field programmable gate arrays FPGAs are one of the most famous architecture families of reconfigurable devices FPGAs can be seen as arrays of logic units that can be reconfigured to realize any digital systems Their high versatility has enabled designers to drastically reduce time to market and made FPGAs suitable for prototyping or small production series in many branches of industrial products In addition and

thanks to innovations at the architecture level FPGAs are now conquering segments of mass markets such as mobile communications Reconfigurable Logic Architecture Tools and Applications offers a snapshot of the state of the art of reconfigurable logic systems Covering a broad range of architectures tools and applications this book Explores classical FPGA architectures and their supporting tools Evaluates recent proposals related to FPGA architectures including the use of network on chips NoCs Examines reconfigurable processors that merge concepts borrowed from the reconfigurable domain into processor design Exploits FPGAs for high performance systems efficient error correction codes and high bandwidth network routers with built in security Expounds on emerging technologies to enhance FPGA architectures improve routing structures and create non volatile configuration flip flops Reconfigurable Logic Architecture Tools and Applications reviews current trends in reconfigurable platforms providing valuable insight into the future potential of reconfigurable systems

Handbook of Wafer Bonding Peter Ramm,James Jian-Qiang Lu,Maaike M. V. Taklo,2012-02-13 The focus behind this book on wafer bonding is the fast paced changes in the research and development in three dimensional 3D integration temporary bonding and micro electro mechanical systems MEMS with new functional layers Written by authors and edited by a team from microsystems companies and industry near research organizations this handbook and reference presents dependable first hand information on bonding technologies Part I sorts the wafer bonding technologies into four categories Adhesive and Anodic Bonding Direct Wafer Bonding Metal Bonding and Hybrid Metal Dielectric Bonding Part II summarizes the key wafer bonding applications developed recently that is 3D integration MEMS and temporary bonding to give readers a taste of the significant applications of wafer bonding technologies This book is aimed at materials scientists semiconductor physicists the semiconductor industry IT engineers electrical engineers and libraries

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