

Shichun Qu · Yong Liu

Wafer-Level Chip-Scale Packaging

Analog and Power Semiconductor
Applications

 Springer

Wafer Level Chip Scale Packaging Analog And Power Semiconductor Applications

Wolfgang Guggemos



Wafer Level Chip Scale Packaging Analog And Power Semiconductor Applications:

Wafer-Level Chip-Scale Packaging Shichun Qu,Yong Liu,2014-09-10 Analog and Power Wafer Level Chip Scale Packaging presents a state of art and in depth overview in analog and power WLCSP design material characterization reliability and modeling Recent advances in analog and power electronic WLCSP packaging are presented based on the development of analog technology and power device integration The book covers in detail how advances in semiconductor content analog and power advanced WLCSP design assembly materials and reliability have co enabled significant advances in fan in and fan out with redistributed layer RDL of analog and power device capability during recent years Since the analog and power electronic wafer level packaging is different from regular digital and memory IC package this book will systematically introduce the typical analog and power electronic wafer level packaging design assembly process materials reliability and failure analysis and material selection Along with new analog and power WLCSP development the role of modeling is a key to assure successful package design An overview of the analog and power WLCSP modeling and typical thermal electrical and stress modeling methodologies is also presented in the book **Power Electronic Packaging** Yong Liu,2012-02-15 Power Electronic Packaging presents an in depth overview of power electronic packaging design assembly reliability and modeling Since there is a drastic difference between IC fabrication and power electronic packaging the book systematically introduces typical power electronic packaging design assembly reliability and failure analysis and material selection so readers can clearly understand each task s unique characteristics Power electronic packaging is one of the fastest growing segments in the power electronic industry due to the rapid growth of power integrated circuit IC fabrication especially for applications like portable consumer home computing and automotive electronics This book also covers how advances in both semiconductor content and power advanced package design have helped cause advances in power device capability in recent years The author extrapolates the most recent trends in the book s areas of focus to highlight where further improvement in materials and techniques can drive continued advancements particularly in thermal management usability efficiency reliability and overall cost of power semiconductor solutions [Handbook of 3D Integration, Volume 3](#) Philip Garrou,Mitsumasa Koyanagi,Peter Ramm,2014-04-22 Edited by key figures in 3D integration and written by top authors from high tech companies and renowned research institutions this book covers the intricate details of 3D process technology As such the main focus is on silicon via formation bonding and debonding thinning via reveal and backside processing both from a technological and a materials science perspective The last part of the book is concerned with assessing and enhancing the reliability of the 3D integrated devices which is a prerequisite for the large scale implementation of this emerging technology Invaluable reading for materials scientists semiconductor physicists and those working in the semiconductor industry as well as IT and electrical engineers *Advances in Semiconductor Technologies* An Chen,2022-10-11 Advances in Semiconductor Technologies Discover the broad sweep of semiconductor technologies in this

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McGraw-Hill Yearbook of Science and Technology, 2010 McGraw-Hill,2009-12-22 More than 150 articles explore the latest advances in science and technology For more than 45 years this annual publication has made information on the latest trends and developments in science and technology accessible to non specialists through concise well illustrated articles Readers will find 150 articles from 200 leaders in their respective fields covering disciplines from Astronomy to Zoology The Yearbook will be of interest to students writers researchers professionals and general readers **Fan-Out**

Wafer-Level Packaging John H. Lau,2018-04-05 This comprehensive guide to fan out wafer level packaging FOWLP technology compares FOWLP with flip chip and fan in wafer level packaging It presents the current knowledge on these key enabling technologies for FOWLP and discusses several packaging technologies for future trends The Taiwan Semiconductor Manufacturing Company TSMC employed their InFO integrated fan out technology in A10 the application processor for Apple s iPhone in 2016 generating great excitement about FOWLP technology throughout the semiconductor packaging community For many practicing engineers and managers as well as scientists and researchers essential details of FOWLP such as the temporary bonding and de bonding of the carrier on a reconstituted wafer panel epoxy molding compound EMC dispensing compression molding Cu revealing RDL fabrication solder ball mounting etc are not well understood Intended to help readers learn the basics of problem solving methods and understand the trade offs inherent in making system level decisions quickly this book serves as a valuable reference guide for all those faced with the challenging problems created by the ever increasing interest in FOWLP helps to remove roadblocks and accelerates the design materials process and manufacturing development of key enabling technologies for FOWLP **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1997

ASM Handbook ASM International. Handbook Committee,2000 This index eliminates that need to search through multiple back of the book indexes to find where a subject is addressed The A to Z listing will help users find important handbook content in volumes where they may not have thought to look **Signals** ,1991

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