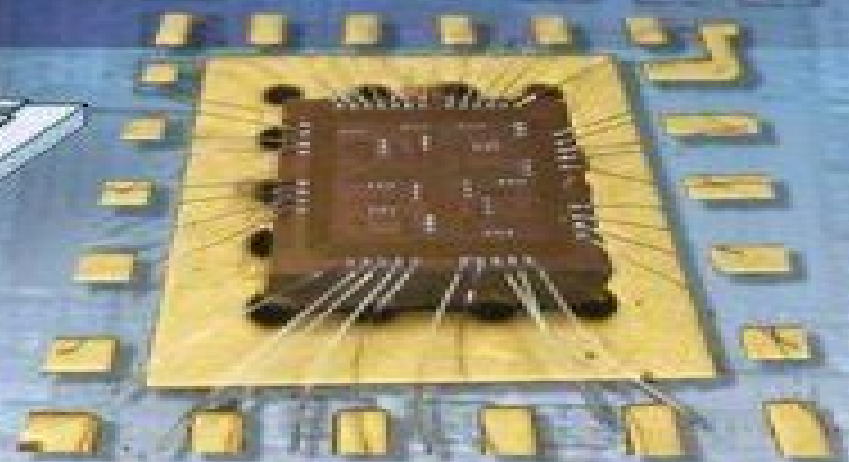
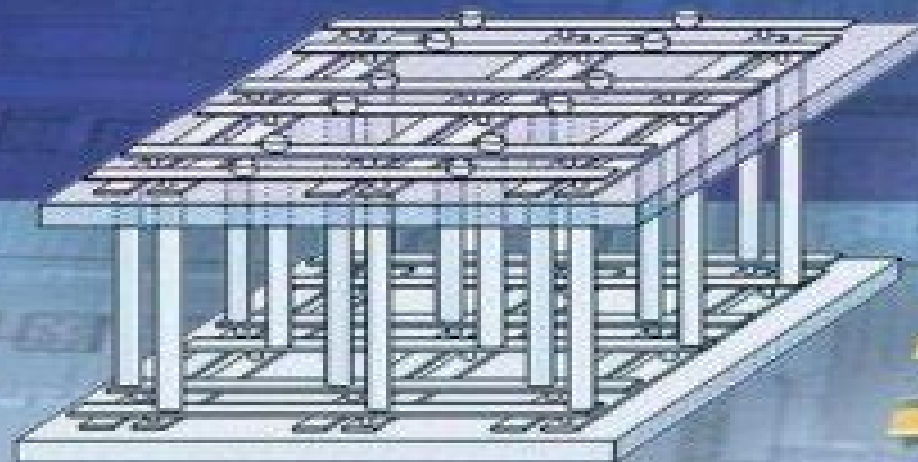
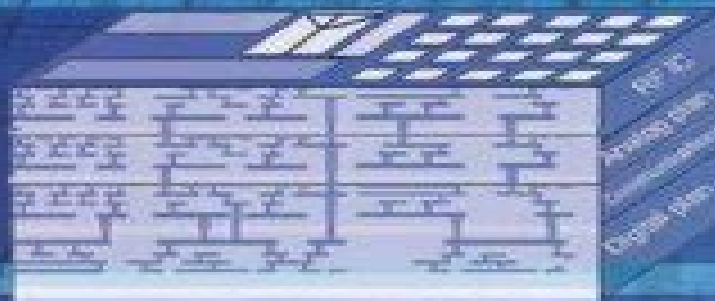




THREE-DIMENSIONAL INTEGRATED CIRCUIT DESIGN

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Three Dimensional Integrated Circuit Design Systems On Silicon

Rohit Sharma

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Three Dimensional Integrated Circuit Design Systems On Silicon:

Three-dimensional Integrated Circuit Design Vasilis F. Pavlidis, Eby G. Friedman, 2010-07-28 With vastly increased complexity and functionality in the nanometer era i.e. hundreds of millions of transistors on one chip increasing the performance of integrated circuits has become a challenging task Connecting effectively interconnect design all of these chip elements has become the greatest determining factor in overall performance 3 D integrated circuit design may offer the best solutions in the near future This is the first book on 3 D integrated circuit design covering all of the technological and design aspects of this emerging design paradigm while proposing effective solutions to specific challenging problems concerning the design of 3 D integrated circuits A handy comprehensive reference or a practical design guide this book provides a sound foundation for the design of 3 D integrated circuits Demonstrates how to overcome interconnect bottleneck with 3 D integrated circuit design leading edge design techniques offer solutions to problems performance power consumption price faced by all circuit designers The FIRST book on 3 D integrated circuit design provides up to date information that is otherwise difficult to find Focuses on design issues key to the product development cycle good design plays a major role in exploiting the implementation flexibilities offered in the 3 D Provides broad coverage of 3 D integrated circuit design including interconnect prediction models thermal management techniques and timing optimization offers practical view of designing 3 D circuits

Three-Dimensional Integrated Circuit Design Yuan Xie, Jingsheng Jason Cong, Sachin Sapatnekar, 2009-12-02 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore's law This observation stated that transistor density in integrated circuits doubles every 1.5-2 years This came with the simultaneous improvement of individual device performance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore's law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device static currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with multiple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be efficiently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs

Three-Dimensional Integrated Circuit Design Vasilis F. Pavlidis, Ioannis Savidis, Eby G. Friedman, 2017-07-04 *Three Dimensional Integrated Circuit Design Second Edition* expands the original with more than twice as much new content adding the latest developments in circuit models temperature

considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization

Three-Dimensional Integrated Circuit Design Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2010-05-19 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs

Design of 3D Integrated Circuits and Systems Rohit Sharma,2018-09-03 Three dimensional 3D integration of microsystems and subsystems has become essential to the future of semiconductor technology development 3D integration requires a greater understanding of several interconnected systems stacked over each other While this vertical growth profoundly increases the system functionality it also exponentially increases the design complexity Design of 3D Integrated Circuits and Systems tackles all aspects of 3D integration including 3D circuit and system design new processes and simulation techniques alternative communication schemes for 3D circuits and systems application of novel materials for 3D

systems and the thermal challenges to restrict power dissipation and improve performance of 3D systems. Containing contributions from experts in industry as well as academia, this authoritative text illustrates different 3D integration approaches such as die-to-die, die-to-wafer, and wafer-to-wafer. It discusses the use of interposer technology and the role of Through-Silicon Vias (TSVs). It presents the latest improvements in three major fields of thermal management for multiprocessor systems on chip (MPSoCs). It explores ThruChip Interface (TCI) NAND flash memory stacking and emerging applications. It describes large-scale integration testing and state-of-the-art low-power testing solutions. Complete with experimental results of chip-level 3D integration schemes tested at IBM and case studies on advanced complementary metal-oxide-semiconductor (CMOS) integration for 3D integrated circuits (ICs), *Design of 3D Integrated Circuits and Systems* is a practical reference that not only covers a wealth of design issues encountered in 3D integration but also demonstrates their impact on the efficiency of 3D systems.

VLSI-SoC: Design Methodologies for SoC and SiP Christian Piguet, Ricardo Reis, Dimitrios Soudris, 2010-04-06

This book contains extended and revised versions of the best papers that were presented during the 16th edition of the IFIP IEEE WG10.5 International Conference on Very Large Scale Integration: A Global System on a Chip Design (CAD) conference. The 16th conference was held at the Grand Hotel of Rhodes Island, Greece, October 13-15, 2008. Previous conferences have taken place in Edinburgh, Trondheim, Vöcklabruck, Munich, Grenoble, Tokyo, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice, and Atlanta. VLSI SoC 2008 was the 16th in a series of international conferences sponsored by IFIP TC 10 Working Group 10.5 and IEEE CEDA that explores the state of the art and the new developments in the field of VLSI systems and their designs. The purpose of the conference was to provide a forum to exchange ideas and to present industrial and research results in the fields of VLSI, ULSI, systems, embedded systems, and microelectronic design and test.

Physical Design for 3D Integrated Circuits Aida Todri-Sanial, Chuan Seng Tan, 2017-12-19

Physical Design for 3D Integrated Circuits reveals how to effectively and optimally design 3D integrated circuits (ICs). It also analyzes the design tools for 3D circuits while exploiting the benefits of 3D technology. The book begins by offering an overview of physical design challenges with respect to conventional 2D circuits, and then each chapter delivers an in-depth look at a specific physical design topic. This comprehensive reference contains extensive coverage of the physical design of 2.5D, 3D ICs, and monolithic 3D ICs. It supplies state-of-the-art solutions for challenges unique to 3D circuit design. Features contributions from renowned experts in their respective fields. *Physical Design for 3D Integrated Circuits* provides a single convenient source of cutting-edge information for those pursuing 2.5D, 3D technology.

Proceedings of International Conference on Frontiers in Computing and Systems Debotosh Bhattacharjee, Dipak Kumar Kole, Nilanjan Dey, Subhadip Basu, Dariusz Plewczynski, 2020-11-23

This book gathers outstanding research papers presented at the International Conference on Frontiers in Computing and Systems (COMSYS 2020) held on January 13-15, 2019, at Jalpaiguri Government Engineering College, West Bengal, India, and jointly organized by the Department of Computer Science Engineering and Department of Electronics Communication Engineering.

The book presents the latest research and results in various fields of machine learning computational intelligence VLSI networks and systems computational biology and security making it a rich source of reference material for academia and industry alike

Three Dimensional System Integration Antonis Papanikolaou,Dimitrios Soudris,Riko Radojcic,2010-12-07 Three dimensional 3D integrated circuit IC stacking is the next big step in electronic system integration It enables packing more functionality as well as integration of heterogeneous materials devices and signals in the same space volume This results in consumer electronics e g mobile handheld devices which can run more powerful applications such as full length movies and 3D games with longer battery life This technology is so promising that it is expected to be a mainstream technology a few years from now less than 10 15 years from its original conception To achieve this type of end product changes in the entire manufacturing and design process of electronic systems are taking place This book provides readers with an accessible tutorial on a broad range of topics essential to the non expert in 3D System Integration It is an invaluable resource for anybody in need of an overview of the 3D manufacturing and design chain

[3D Interconnect Architectures for Heterogeneous Technologies](#) Lennart Bamberg,Jan Moritz Joseph,Alberto García-Ortiz,Thilo Pionteck,2022-06-27 This book describes the first comprehensive approach to the optimization of interconnect architectures in 3D systems on chips SoCs specially addressing the challenges and opportunities arising from heterogeneous integration Readers learn about the physical implications of using heterogeneous 3D technologies for SoC integration while also learning to maximize the 3D technology gains through a physical effect aware architecture design The book provides a deep theoretical background covering all abstraction levels needed to research and architect tomorrow s 3D integrated circuits an extensive set of optimization methods for power performance area and yield as well as an open source optimization and simulation framework for fast exploration of novel designs

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design

Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

Wafer Level 3-D ICs Process Technology Chuan Seng Tan,Ronald J. Gutmann,L. Rafael Reif,2009-06-29 Three dimensional 3D integration is clearly the simplest answer to most of the semiconductor industry s vexing problems heterogeneous integration and reductions of power form factor delay and even cost Conceptually the power latency and form factor of a system with a fixed number of transistors all scale roughly linearly with the diameter of the smallest sphere enclosing frequently interacting devices This clearly provides the fundamental motivation behind 3D technologies which vertically stack several strata of device and interconnect layers with high vertical interconnectivity In addition the ability to vertically stack strata with divergent and even incompatible process flows provides for low cost and low parasitic integration of diverse technologies such as sensors energy scavengers nonvolatile memory dense memory fast memory processors and RF layers These capabilities coupled with today s trends of increasing levels of integrated functionality lower power smaller form factor increasingly divergent process flows and functional diversification would seem to make 3D technologies a natural choice for most of the semiconductor industry Since the concept of vertical integration of different strata has been around for over 20 years why aren t vertically stacked strata endemic to the semiconductor industry The simple answer to this question is that in the past the 3D advantages while interesting were not necessary due to the tremendous opportunities offered by geometric scaling In addition even when the global interconnect problem of high performance single core processors seemed insurmountable without innovations such as 3D alternative architectural solutions such as multicores could effectively delay but not eliminate the need for 3D

Three-Dimensional Design Methodologies for Tree-based FPGA Architecture Vinod Pangracious,Zied Marrakchi,Habib Mehrez,2015-06-25 This book focuses on the development of 3D design and implementation methodologies for Tree based FPGA architecture It also stresses the needs for new and augmented 3D CAD tools to support designs such as the design for 3D to manufacture high performance 3D integrated circuits and reconfigurable FPGA based systems This book was written as a text that covers the foundations of 3D integrated system design and FPGA architecture design It was written for the use in an elective or core course at the graduate level in field of Electrical Engineering Computer Engineering and Doctoral Research programs No previous background on 3D integration is required nevertheless fundamental understanding of 2D CMOS VLSI design is required It is assumed that reader has taken the core curriculum in Electrical Engineering or Computer Engineering with courses like CMOS VLSI design Digital System Design and Microelectronics Circuits being the most important It is accessible for self study by both senior students and professionals alike

Nano-Semiconductors Krzysztof Iniewski,2018-09-03 With contributions from top international experts from both industry and academia Nano Semiconductors Devices and Technology is a must read for anyone with a serious interest in future nanofabrication technologies Taking into account the semiconductor industry s

transition from standard CMOS silicon to novel device structures including carbon nanotubes CNT graphene quantum dots and III V materials this book addresses the state of the art in nano devices for electronics It provides an all encompassing one stop resource on the materials and device structures involved in the evolution from micro to nanoelectronics The book is divided into three parts that address Semiconductor materials i e carbon nanotubes memristors and spin organic devices Silicon devices and technology i e BiCMOS SOI various 3D integration and RAM technologies and solar cells Compound semiconductor devices and technology This reference explores the groundbreaking opportunities in emerging materials that will take system performance beyond the capabilities of traditional CMOS based microelectronics Contributors cover topics ranging from electrical propagation on CNT to GaN HEMTs technology and applications Approaching the trillion dollar nanotech industry from the perspective of real market needs and the repercussions of technological barriers this resource provides vital information about elemental device architecture alternatives that will lead to massive strides in future development

Arbitrary Modeling of TSVs for 3D Integrated Circuits Khaled Salah, Yehea Ismail, Alaa El-Rouby, 2014-08-21 This book presents a wide band and technology independent SPICE compatible RLC model for through silicon vias TSVs in 3D integrated circuits This model accounts for a variety of effects including skin effect depletion capacitance and nearby contact effects Readers will benefit from in depth coverage of concepts and technology such as 3D integration Macro modeling dimensional analysis and compact modeling as well as closed form equations for the through silicon via parasitics Concepts covered are demonstrated by using TSVs in applications such as a spiral inductor and inductive based communication system and bandpass filtering

Analyse Et Caractérisation Des Couplages Substrat Et de la Connectique Dans Les Circuits 3D Fengyuan Sun, 2016 The proposal of doubling the number of transistors on an IC chip with minimum costs and subtle innovations every 24 months by Gordon Moore in 1965 the so called Moore's law has been the most powerful driver for the emphasis of the microelectronics industry in the past 50 years This law enhances lithography scaling and integration in 2D of all functions on a single chip increasingly through system on chip SOC On the other hand the integration of all these functions can be achieved through 3D integrations Generally speaking 3D integration consists of 3D IC packaging 3D IC integration and 3D Si integration They are different and mostly the TSV through silicon via separates 3D IC packaging from 3D IC Si integrations since the latter two uses TSVs but 3D IC packaging does not TSV with a new concept that every chip or interposer could have two surfaces with circuits is the heart of 3D IC Si integrations Continued technology scaling together with the integration of disparate technologies in a single chip means that device performance continues to outstrip interconnect and packaging capabilities and hence there exist many difficult engineering challenges most notably in power management noise isolation and intra and inter chip communication 3D Si integration is the right way to go and compete with Moore's law more than Moore versus more Moore However it is still a long way to go In this book Fengyuan SUN proposes new substrate network extraction techniques Using this latter the substrate coupling and loss in IC's can be

analyzed He implements some Green TLM Transmission Line Matrix algorithms in MATLAB It permits to extract impedances between any number of embedded contacts or and TSVs He does investigate models of high aspect ratio TSV on both analytical and numerical methods electromagnetic simulations This model enables to extract substrate and TSV impedance S parameters and parasitic elements considering the variable resistivity of the substrate It is full compatible with SPICE like solvers and should allow an investigation in depth of TSV impact on circuit performance Designing TSVs for 3D

Integrated Circuits Nauman Khan, Soha Hassoun, 2012-09-22 This book explores the challenges and presents best strategies for designing Through Silicon Vias TSVs for 3D integrated circuits It describes a novel technique to mitigate TSV induced noise the GND Plug which is superior to others adapted from 2 D planar technologies such as a backside ground plane and traditional substrate contacts The book also investigates in the form of a comparative study the impact of TSV size and granularity spacing of C4 connectors off chip power delivery network shared and dedicated TSVs and coaxial TSVs on the quality of power delivery in 3 D ICs The authors provide detailed best design practices for designing 3 D power delivery networks Since TSVs occupy silicon real estate and impact device density this book provides four iterative algorithms to minimize the number of TSVs in a power delivery network Unlike other existing methods these algorithms can be applied in early design stages when only functional block level behaviors and a floorplan are available Finally the authors explore the use of Carbon Nanotubes for power grid design as a futuristic alternative to Copper **Noise Coupling in**

System-on-Chip Thomas Noulis, 2018-01-09 Noise Coupling is the root cause of the majority of Systems on Chip SoC product fails The book discusses a breakthrough substrate coupling analysis flow and modelling toolset addressing the needs of the design community The flow provides capability to analyze noise components propagating through the substrate the parasitic interconnects and the package Using this book the reader can analyze and avoid complex noise coupling that degrades RF and mixed signal design performance while reducing the need for conservative design practices With chapters written by leading international experts in the field novel methodologies are provided to identify noise coupling in silicon It additionally features case studies that can be found in any modern CMOS SoC product for mobile communications automotive applications and readout front ends Advanced Interconnects for ULSI Technology Mikhail Baklanov, Paul S.

Ho, Ehrenfried Zschech, 2012-04-02 Finding new materials for copper low k interconnects is critical to the continuing development of computer chips While copper low k interconnects have served well allowing for the creation of Ultra Large Scale Integration ULSI devices which combine over a billion transistors onto a single chip the increased resistance and RC delay at the smaller scale has become a significant factor affecting chip performance Advanced Interconnects for ULSI Technology is dedicated to the materials and methods which might be suitable replacements It covers a broad range of topics from physical principles to design fabrication characterization and application of new materials for nano interconnects and discusses Interconnect functions characterisations electrical properties and wiring requirements Low k materials

fundamentals advances and mechanical properties Conductive layers and barriers Integration and reliability including mechanical reliability electromigration and electrical breakdown New approaches including 3D optical wireless interchip and carbon based interconnects Intended for postgraduate students and researchers in academia and industry this book provides a critical overview of the enabling technology at the heart of the future development of computer chips *Interconnect Technologies for Integrated Circuits and Flexible Electronics* Yash Agrawal,Kavicharan Mummaneni,P. Uma Sathyakam,2023-09-21 This contributed book provides a thorough understanding of the basics along with detailed state of the art emerging interconnect technologies for integrated circuit design and flexible electronics It focuses on the investigation of advanced on chip interconnects which match the current as well as future technology requirements The contents focus on different aspects of interconnects such as material physical characteristics parasitic extraction design structure modeling machine learning and neural network based models for interconnects signaling schemes varying signal integrity performance analysis variability reliability aspects associated electronic design automation tools The book also explores interconnect technologies for flexible electronic systems It also highlights the integration of sensors with stretchable interconnects to demonstrate the concept of a stretchable sensing network for wearable and flexible applications This book is a useful guide for those working in academia and industry to understand the fundamentals and application of interconnect technologies

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