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Transient and Permanent Error Control for Networks-on-Chip

Transient And Permanent Error Control For Networks On Chip

**Érika Cota,Alexandre de Moraes
Amory,Marcelo Soares Lubaszewski**



Transient And Permanent Error Control For Networks On Chip:

Transient and Permanent Error Control for Networks-on-Chip Qiaoyan Yu, Paul Ampadu, 2011-11-18 This book addresses reliability and energy efficiency of on chip networks using cooperative error control It describes an efficient way to construct an adaptive error control codec capable of tracking noise conditions and adjusting the error correction strength at runtime Methods are also presented to tackle joint transient and permanent error correction exploiting the redundant resources already available on chip A parallel and flexible network simulator is also introduced which facilitates examining the impact of various error control methods on network on chip performance *Transient and Permanent Error Control for*

Networks-On-Chip Springer, 2012-05-01

Error Control for Network-on-Chip Links Bo Fu, Paul Ampadu, 2011-10-09

This book provides readers with a comprehensive review of the state of the art in error control for Network on Chip NOC links Coverage includes detailed description of key issues in NOC error control faced by circuit and system designers as well as practical error control techniques to minimize the impact of these errors on system performance *Reliability,*

Availability and Serviceability of Networks-on-Chip Érika Cota, Alexandre de Moraes Amory, Marcelo Soares

Lubaszewski, 2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the art on chip communication architectures **Asynchronous On-Chip Networks and Fault-Tolerant Techniques** Wei

Song, Guangda Zhang, 2022-05-10 Asynchronous On Chip Networks and Fault Tolerant Techniques is the first comprehensive study of fault tolerance and fault caused deadlock effects in asynchronous on chip networks aiming to overcome these drawbacks and ensure greater reliability of applications As a promising alternative to the widely used synchronous on chip networks for multicore processors asynchronous on chip networks can be vulnerable to faults even if they can deliver the same performance with much lower energy and area compared with their synchronous counterparts faults can not only corrupt data transmission but also cause a unique type of deadlock By adopting a new redundant code along with a dynamic fault detection and recovery scheme the authors demonstrate that asynchronous on chip networks can be efficiently hardened to tolerate both transient and permanent faults and overcome fault caused deadlocks This book will serve as an essential guide for researchers and students studying interconnection networks fault tolerant computing asynchronous system design circuit design and on chip networking as well as for professionals interested in designing fault tolerant and high throughput asynchronous circuits Transient and Permanent Error Management for Networks-on-chip Qiaoyan

Yu, 2011 Reliability has become one of the most important metrics for on chip communications infrastructures in nanoscale technologies Reduced supply voltages and high clock frequency exacerbate the impact of noise sources such as particle strikes and crosstalk which can cause transient errors in transmitted data Manufacturing defects and aging issues can cause

permanent errors in the communication links The modularity of the Networks on Chip NoCs approach facilitates the exploration of error control techniques for on chip interconnects and many cores systems Unfortunately error control is not free Worst case error management methods are simple but waste energy and bandwidth in favorable noise conditions Consequently cost effective techniques for improving link error resilience are needed In this work we propose configurable error control methods to tackle variable transient errors and exploit existing transient error control redundancy for permanent error management achieving high reliability and low average energy consumption with minor area overhead To adapt to the variable transient error rates a configurable error control coding ECC scheme is proposed for datalink layer transient error management The proposed method can adjust both error detection and error correction capability at runtime by varying the number of redundant wires for parity check bits The obtained error resilience makes the proposed method suitable for a range of link error rates Configuring the number of redundant wires to match the noise conditions reduces the average energy consumption in the ECC codec and interconnect link A hardware efficient implementation for the configurable ECC is presented as well We integrate the error control techniques in the datalink and physical layers to co manage transient and permanent errors Infrequently used redundant wires for the configurable ECC are utilized as spare wires to replace permanently unusable links To maintain the transient and permanent error co management capability as noise conditions change we propose a packet re organization algorithm combined with shortening error control coding method This method reduces the need for energy consuming fault tolerant routing minimizing latency and energy overhead induced by error control This co management method is suitable for NoCs operating in variable noise conditions with a small number of permanently unusable wires To further improve energy efficiency the adaptation on ECC is extended to the network layer We employ end to end error control in the network layer in low noise conditions and enhance the error control capability in high noise conditions by adding hop to hop error control in the datalink layer A protocol that boosts or reduces error control strength is presented to support runtime seamless ECC mode switching Simply combining end to end error control with hop to hop error control significantly increases energy consumption To address this issue we apply the concept of product codes to the dual layer error control the hop to hop error control is designed to be compatible with one dimension of the product code Consequently the dual layer cooperative error control can switch error control modes without interrupting normal NoC operation achieving high reliability and energy efficiency in a wide range of link error rates To evaluate performance and energy consumption of different error control methods on a large size NoC we propose a flexible parallel NoC simulator Plug and play error control coding ECC insertion and some typical error control codecs have been implemented in the simulator The flexible fault injection environment provided by our simulator assists error control exploration for specific purposes In addition we use C and message passing interface MPI languages to schedule parallel simulation on a multiprocessor server addressing the prohibitive simulation time and system resource challenges caused by

the large number of communicating nodes and extensive number of simulation variables Leaves iv vi Network-on-Chip
Santanu Kundu, Santanu Chattopadhyay, 2018-09-03 Addresses the Challenges Associated with System on Chip Integration
Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3 D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

Reconfigurable Networks-on-Chip Sao-Jie Chen, Ying-Cherng Lan, Wen-Chung Tsai, Yu-Hen Hu, 2011-12-16 This book provides a comprehensive survey of recent progress in the design and implementation of Networks on Chip It addresses a wide spectrum of on chip communication problems ranging from physical network to application layers Specific topics that are explored in detail include packet routing resource arbitration error control correction application mapping and communication scheduling Additionally a novel bi directional communication channel NoC BiNoC architecture is described with detailed explanation Written for practicing engineers in need of practical knowledge about the design and implementation of networks on chip Includes tutorial like details to introduce readers to a diverse range of NoC designs as well as in depth analysis for designers with NoC experience to explore advanced issues Describes a variety of on chip

communication architectures including a novel bi directional communication channel NoC From the Foreword Overall this book shows important advances over the state of the art that will affect future system design as well as R D in tools and methods for NoC design It represents an important reference point for both designers and electronic design automation researchers and developers Giovanni De Micheli **Designing 2D and 3D Network-on-Chip Architectures** Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies **'Advances in Microelectronics: Reviews', Vol_1** Sergey Yurish,2017-12-24 The 1st volume of Advances in Microelectronics Reviews Book Series contains 19 chapters written by 72 authors from academia and industry from 16 countries With unique combination of information in each volume the Advances in Microelectronics Reviews Book Series will be of value for scientists and engineers in industry and at universities In order to offer a fast and easy reading of the state of the art of each topic every chapter in this book is independent and self contained All chapters have the same structure first an introduction to specific topic under study second particular field description including sensing applications Each of chapter is ending by well selected list of references with books journals conference proceedings and web sites This book ensures that readers will stay at the cutting edge of the field and get the right and effective start point and road map for the further researches and developments

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